DEVELOPMENT OF III-NITRIDE TRANSISTORS: HETEROJUNCTION BIPOLAR TRANSISTORS AND FIELD-EFFECT TRANSISTORS

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LIST OF SYMBOLS AND ABBREVIATIONS

$\Delta V_{hysteresis}$	I-V hysteresis
ΔV_{th}	Threshold voltage shifting
ΔE_c	Conduction band energy difference
ΔE_g	Bandgap difference
β	Common-emitter d.c. current gain
μ	Carrier mobility
ρ_c	Specific contact resistance
σ_{int}	Charged interface trap density
σ_P	Polarization-induced charge density
τ_b	Neutral base transit time
τ_c	Collector charging time
τ_e	Emitter charging time
τ_{ec}	Emitter-collector transit time
τ_{sc}	BC junction space-charge transit time
ϕ_B	Schottky barrier height
2DEG	Two-dimensional electron gas
ADS	Advance Design System
A_E	Emitter area
AFM	Atomic force microscope
ALD	Atomic-layer deposition
AlGaN	Aluminum gallium nitride
AlN	Aluminum nitride
$AlON_x$	Aluminum oxynitride
APD	Avalanche photo-detector
BC	Base-collector
BCB	Benzocyclobutene
BCl_3	Boron trichloride
BFoM	Baliga's Figure of Merit
BOE	Buffered oxide etchant
BV_{CBO}	Collector-to-base breakdown voltage with the emitter open circuited
BV_{CEO}	Collector-to-emitter breakdown voltage with the base open circuited
C_{gg}	Gate capacitance
C_{jc}	Junction capacitance of the base-collector junction
C_{je}	Junction capacitance of the base-emitter junction
C_m	Measured capacitance

CPW	Coplanar waveguide
C_Q	Quantum capacitance
C-V	Capacitance-voltage
d.c	Direct current
DG-HBT	Direct-growth heterojunction bipolar transistor
D_{it}	Trap density
DLOS	Deep-level optical spectroscopy
DLTS	Deep-level transient spectroscopy
D_{nB}	Electron diffusion coefficient in base layer
DOE	Design of experiment
D_{pE}	Hole diffusion coefficient in emitter layer
E-gun	Electron-gun
E_A	Trap activation energy level
EBL	Electron blocking layer
E_C	Conduction band energy level
E_i	Effect estimates
E_{photon}	Photon energy
E_{trap}	Trap energy level
f_{max}	Maximum oscillation frequency
FS-GaN	Free-standing gallium nitride
f_T	Unity current gain frequency
GaAs	Gallium arsenide
GaN	Gallium nitride
Ga-polar	Gallium-polar
Ge	Germanium
g_m	Transconductance
GS	Gate-to-source
HBT	Heterojunction bipolar transistor
HEMT	High-electron-mobility transistor
HfAlO	Hafnium aluminum oxide
h_{fe}	Differential current gain
HFET	Heterojunction field-effect transistor
high-*k*	High dielectric constant
I_B	Base current
$I_{B,bulk}$	Bulk recombination current in neutral base region
$I_{B,scr}$	Recombination current in BE space-charge region
I_{Bp}	Back-injected base current
I_{Br}	Base recombination current
I_C	Collector current
I_{Cn}	Electron current of BC junction

ICP	Inductive-coil-plasma
$I_{D,max}$	Maximum drain current
I_E	Emitter current
I_{En}	Electron current of BE junction
I_{GS}	Gate-to-source current
III-N	III-Nitride
I_n	Normalized drain current
InAlN	Indium aluminum nitride
InGaAs	Indium gallium arsenide
InGaN	Indium gallium nitride
InGaP	Indium gallium phosphide
InN	Indium nitride
InP	Indium phosphide
IR	Infrared
I-V	Current-voltage
J_{area}	Area-dependent current component
J_C	Emitter current density
JFET	Junction field-effect transistor
JFoM	Johnson's figure of merit
$K_2S_2O_8$	Potassium persulfate
$K_{B,cont}$	Interface recombination current at the base contacts
$K_{B,surf}$	Extrinsic base surface recombination current
KOH	Potassium hydroxide
$K_{perimeter}$	Perimeter-dependent recombination current
LD	Laser diode
L_E	Emitter perimeter
LED	Light-emitting diode
L_G	Gate length
L_{GD}	Gate-to-drain distance
L_{GS}	Gate-to-source distance
LM	Lattice-matched
MAG	Maximum available gain
MESFET	Metal–semiconductor field-effect transistor
MIS	Metal-insulator-semiconductor
MISFET	Metal-insulator-semiconductor field-effect transistor
MMIC	Monolithic microwave integrated circuit
MOCVD	Metalorganic chemical vapor deposition
N_B	Free-carrier density of base layer
n_C	Free-electron concentration of collector layer
N_E	Free-carrier density of emitter layer

N_{ox}	Fixed oxide charge density
N-polar	Nitrogen-polar
n_s	Sheet electron density
P	Total polarization
p_B	Free-hole concentration of base layer
P_{dc}	Power density
PE-ALD	Plasma-enhanced atomic-layer deposition
PE-CVD	Plasma-enhanced chemical vapor deposition
PNA	Power network analyzer
P^{PE}	Piezoelectric polarization
P^{SP}	Spontaneous polarization
Q_{trap}	Charged trap density
QW	Quantum well
r_B	Base resistance
r_C	Collector resistance
R_D	Drain resistance
r_E	Emitter resistance
$relax$	Relaxation factor
R_G	Gate resistance
RIE	Reactive ion etching
R_{on}	On-resistance
$R_{ON,DC}$	D.c on-resistance
$R_{ON,dynamic}$	Dynamic on-resistance
R_S	Source resistance
RTA	Rapid thermal annealing
SEM	Scanning electron microscopy
SFP	Source-field plate
Si	Silicon
SiC	Silicon carbide
SiN	Silicon nitride
SOLT	Short-open-load-through
TLM	Transmission-line model
TMA	Trimethylaluminium
U	Mason’s unilateral gain
UID	Unintentionally doped
UV	Ultraviolet
V_{BE}	Base-emitter junction voltage
V_{CE}	Collector-emitter voltage
V_{bi}	Built-in potential
V_{knee}	Knee voltage

VNA	Vector network analyzer
V_{offset}	Offset voltage
V_{th}	Threshold voltage
$V_{th,MIS}$	Threshold voltage of a MIS structure
W_G	Gate width
X_B	Thickness of the base layer
X_{dep}	Base-collector junction depletion width
X_E	Thickness of the emitter layer
XPS	X-ray photoelectron spectroscopy

SUMMARY

This dissertation presents the development and achievement on III-nitride (III-N) heterojunction bipolar transistors (HBTs), heterojunction field-effect transistors (HFETs) and metal-insulator-semiconductor field-effect transistors (MISFETs) developed at Georgia Tech for high-power and microwave applications. The research work focused on the fabrication processes development and device characterization for achieving better device performance and understanding the issues in III-N transistors. Several unique fabrication processes were developed to overcome the challenges for different III-N transistors. Software simulator was also used to explore optimal device designs for III-N transistors. D.c, microwave and quasi-static *I-V* and *C-V* measurements were carried out to characterize the fabricated III-N transistors and diodes.

III-N HBTs are considered as promising devices for the next-generation microwave and power electronics. However, inevitable etching damage and high base resistance are major technical challenges to achieve high-performance III-N HBTs. Using an optimal nitrogen-incorporated dry etching process and Pd-base base contacts, *npn* GaN/InGaN direct-growth HBTs (DG-HBTs) grown on free-standing GaN (FS-GaN) substrates demonstrated a high current gain (h_{fe}) > 110, high current density (J_C) > 141 kA/cm^2, and high power density (P_{dc}) > 3 MW/cm^2. The fabricated GaN/InGaN DG-HBTs also demonstrated the capability to operate at high temperature environment (250 C) with increased breakdown voltage (> 160 V). The first III-N DG-HBT showing f_T > 8 GHz and f_{max} > 1.3 GHz were also measured.

III-N HFETs have also been a focused research topic because of the potential in high current drive and high breakdown voltage. However, resistive ohmic contacts,

normally-on characteristics and a high density of surface states are the major challenges for III-N HFETs. To address these issues, an in-situ doping technique and a unique electrode-less wet etching processes were developed. The fabricated recessed-gate HFETs demonstrated V_{th} = 0 V with 0.17 V deviation across the sample. Baliga's figure of merit is 240 MW/cm^2 was achieved. To improve the switching performance, a remote-oxygen-plasma treatment was implemented. Current collapse and dynamic on-resistance are reduced by 67% after the plasma treatment. InAlN/GaN microwave HFETs with 150nm T-gate also achieved current density >1.4 A/mm with maximum transconductance (g_m) > 250 mS/mm. The measured f_T achieved 80 GHz and f_{max} > 110 GHz. The $f_T \times L_G$ product is 12 GHz-μm which is among the best results of reported III-N microwave HFETs.

To reduce leakage current in III-N HFETs, a metal-insulator-semiconductor (MIS) gate structure with a high-*k* gate insulator was studied. However, a high density of oxide charge, high gate leakage current and large *I-V* hysteresis are typically observed if the ALD deposition process is not optimized. To obtain an optimal ALD deposition, a 2-level fractional factorial design of experiment (2^{6-2} DOE) was performed. The fabricated normally-on MISFETs showed a minimal V_{th} shifting (< 5 V), small leakage current (< 1 pA/mm), and small hysteresis (< 0.5 V). The vertical breakdown field of the gate insulator is > 5 MV/cm and the lateral breakdown field of MISFETs is > 1.1 MV/cm which are close to the ideal values. Normally-off recessed-gate MISFETs with V_{th} = 0.9 V were also fabricated with the remote-oxygen-plasma treatment. Low leakage current (< 1 pA/mm), high on-off ratio (> 2.2E11), and low sub-threshold voltage slope (< 85 mV/mm) are achieved. The drain current transient spectroscopy revealed 6 common traps

in recessed-gate HFETs and MISFETs with τ = 180 s to 3 ms. A particular trap with τ = 15 s was only observed in MISFETs. The study on recessed-gate MISFETs not only show that the plasma treatment is also beneficial to device performance but also helps to identify the possible source and characteristics of traps in III-N HFETs and MISFETs.

In conclusion, this dissertation covers the complete development and characterization on III-N HBTs, HBTs and MISFETs at Georgia Tech. The results not only indicated the great potential of III-N transistors for high-power and high-frequency applications but also revealed the issues and possible solutions to achieve better performance on III-N transistors.

CHAPTER 1

INTRODUCTION OF III-NITRIDE MATERIALS AND TRANSISTORS

1.1 Properties and applications of III-N materials

III-Nitride (III-N) materials, such as gallium nitride (GaN), aluminum nitride (AlN), indium nitride (InN), and their ternary and quaternary alloys are formed by column-III elements with nitrogen atoms. In recent year, III-N materials become a focused research topic because the great advantage in optoelectronic and high-power applications than other semiconductors. As shown in Table 1, III-N materials possess both the direct bandgap and the wide bandgap ranging from 0.7 eV (InN) to 6.2 eV (AlN). The wide bandgap of GaN and AlN enables the blue and ultraviolet (UV) light-emitting diodes (LEDs) and laser diodes (LDs) for optoelectronic applications. The wide bandgap also provides lower noise than other semiconductors for avalanche photo-detectors (APDs). Using ternary or quaternary III-N alloys with InN, such as InGaN or InAlGaN, smaller bandgap can be achieved for bandgap engineering. This flexibility of bandgap enables the design of optoelectronic devices for light wavelength from UV to infrared (IR.) The bandgap engineering on III-N materials also allows the design of different heterostructure, such as the quantum well (QW) and the electron blocking layer (EBL) to improve the performance of LEDs and LDs.

For electrical applications, the high breakdown field, resulting from the wide bandgap, gives a great advantage to III-N devices over other semiconductors for high-power and high-voltage applications. Passive III-N devices, such as GaN Schottky diodes,

have been intensively studied and commercially available for high-power switching applications. III-N transistors have also been demonstrated with breakdown voltage >1000V. The bandgap engineering on III-N materials also enables the design of heterojunction transistors, such as heterojunction bipolar transistors (HBTs) and heterojunction field-effect transistors (HFETs). In contrary, although silicon carbide (SiC) also has wide bandgap, it does not have the flexibility for bandgap engineering. The good thermal conductivity of III-N materials provides better heat dissipation, which is desirable for high-power optoelectronic and electronic devices. As a result, III-N transistors have been considered as the most promising candidate for the next generation electronic devices.

Table 1 Semiconductor Properties at 300 K [1]

	Binary III-N			Si	Ge	GaAs	InP	4H-SiC
	GaN	AlN	InN					
Lattice Structure	Wurtzite	Wurtzite	Wurtzite	Diamond	Diamond	Zincblende	Zincblende	Wurtzite
Bandgap Energy (eV)	3.189	3.11	2.544	5.431	5.646	5.653	5.869	3.073
Nature of Bandgap	3.44	6.2	0.7 ~ 1.0	1.12	0.66	1.42	1.35	3.26
Breakdown Field (MV/cm)	Direct	Direct	Direct	Indirect	Indirect	Direct	Direct	Indirect
Electron Saturated Velocity (10^7 cm/s)	2.5 ~ 5	1.2 ~ 1.8	NA	0.25 ~ 0.8	0.1	0.3 ~ 0.9	0.5	3 ~ 5
Electron Mobility (cm^2/Vs)	2.5	1.9	3.4	2.3	3.1	0.7	3.9	1.9
Hole Mobility (cm^2/Vs)	1000	300	3200	1400	3900	8000	5400	900
Thermal Conductivity ($W/cm^{-1}K^{-1}$)	400	14	--	500	1900	400	200	120

1.2 Challenges for III-N materials growth and fabrication processes

Although III-N materials have such attractive benefits than other semiconductors, the material epitaxy growth and device fabrication processes are very challenging. For III-N epitaxy growth, the hetero-epitaxial growth on foreign substrates and the strain management in heterostructures are the major challenges. Because of the cost of III-N substrates, III-N materials are usually hetero-epitaxially grown on sapphire, SiC or Si substrates. As shown in Figure 1, the lattice constant (a_0) of III-N materials varies from 3.53Å (InN) to 3.11Å (AlN.) Compared to the lattice constant of sapphire (4.78 Å), SiC (3.08 Å) and Si (5.43 Å), a lattice mismatch is inevitable. A high density of threading dislocations (~10^8 to10^9 cm^{-2}) in epitaxial structures is commonly observed originating from the strained hetero-epitaxial growth on foreign substrates with lattice and thermal mismatches [2]. Those dislocations reduce the performance and lifetime of III-N devices. In addition, a lightly strained III-N heterostructure, such as AlN/GaN, may be preferred for improving device performance. The strain, however, may result in material cracks and defect formation if the growth condition is not well controlled. As a result, the strain management in III-N heterostructures is also very challenging to achieve the desired layer structure with minimal strain-induced defects.

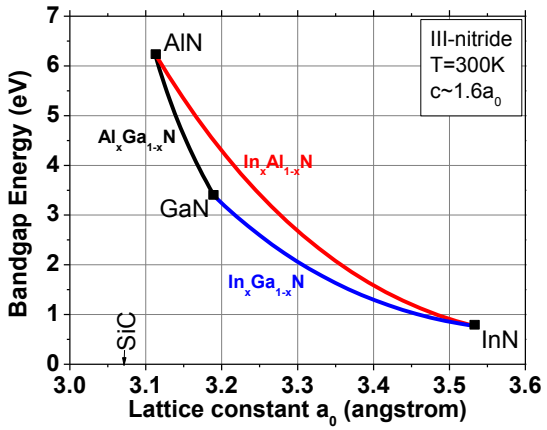

Figure 1. The bandgap and lattice constant of III-N materials [3]

On the other hand, fabrication processes are also challenging. For III-N device fabrication, etching damage, resistive ohmic contacts and a high-density of surface state are typical issues observed on III-N devices. For III-N transistors, these issues severely degrade the achievable device performance. To each III-N materials, plasma-enhanced dry etching techniques in reactive-ion-etching (RIE) or inductive-coil-plasma (ICP) etching tools are typically used [4, 5, 6, 7]. However, nitrogen vacancies [8, 9] or deep level traps [10, 11] in III-N materials are commonly observed on etched surfaces because of inevitable plasma etching damage. Alternatively, photon-enhanced wet etching techniques with electrodes [12] and without electrodes [13, 14] can prevent the plasma damage but these wet etching techniques suffer from non-uniform etching if the process is not well controlled. The etched rough surfaces and sidewalls result in poor device uniformity and contain a high density of surface states. Thus, a uniform low-damage etching process is needed for III-N HBTs and recessed-gate HFETs.

In addition, Schottky rectifying behavior or high contact resistance are commonly observed on the metal contacts of III-N devices because of the wide bandgap of III-N materials. For III-N transistors, resistive contacts significantly limit the achievable current drive and reduce the cut-off frequency. For III-N HBTs, the *p*-type contacts are very challenging because of the inability to achieve highly doped *p*-GaN or *p*-InGaN layers. Ion implantation [15] and selectively regrown contact region for III-N HBTs [16, 17] or III-N HFETs [18, 19] help reduce the contact resistance. However, to reduce the process complexity and cost, direct ohmic contact formation is still preferred. Several different metal stacks and annealing processes have been studied for *n*-type [20, 21] and

p-type contacts [22, 23] However, ohmic contacts still requires further study and optimization to achieve lower resistance.

For III-N transistors, surface passivation and dielectric deposition are also crucial. For III-N HBTs, surface recombination current degrades current gain. Surface states on III-N HFETs and MISFETs have been identified as the major cause of current collapse and gate-lag behavior. Dielectric passivation using PECVD-grown SiN, ALD-grown AlN [24] and HfAlO [25] was reported and showed advantages in the suppression of gate-lag. Surface oxidation using rapid-thermal-oxidation [26], chemical oxidation [27], and UV-Ozone oxidation [28] have been reported to generate a native oxide layer for passivation. However, the quality of the dielectric layer and the abrupt heterogeneous interface between the dielectric layer and III-N surface still affect the leakage current and the stability of III-N HFETs and MISFETs. Therefore, studies on the dielectric deposition on III-N materials [29] and the characterization on dielectric/III-N interfaces [30] have been a very active research area in the past few years. However, a more comprehensive study on the dielectric deposition and interfaces is still required to improve the performance and device stability for III-N HFETs and MISFETs.

In this dissertation, the research work focus on the development and optimization of fabrication processes for different III-N transistors. Several unique fabrication processes were developed to resolve the issues observed in III-N HBTs, HFETs and MISFETs. In the following sections, the up-to-date research results from reported literatures and the achieved device performance at Georgia Tech for III-N HBTs, HFETs and MISFETs will be discussed.

1.3 GaN/InGaN heterojunction bipolar transistors

Compared to FETs with horizontal structure, the vertical structure of HBTs provides higher current density and higher power handling capability, which enables a higher device integration level than FETs. Furthermore, HBTs have the better scaling ability and the normally-off characteristics which are desired for low-power and high-speed circuits. Nowadays, III-V HBTs, such as InP/InGaAs and InGaP/GaAs HBTs, have been important commercial technologies for wireless communication applications because of their ultra-fast switching speed. The reported InP/InGaAs HBT have demonstrated with current-gain cut-off frequency (f_T) larger than 765 GHz at room temperature and 845 GHz at -55 C [31]. The reported power-gain cut-off frequency (f_{max}) reaches larger than 1.1 THz [32]. Nevertheless, the small breakdown voltage, caused by the small bandgap of III-V materials, limits the maximum deliverable power of III-V HBTs.

Because of the wide bandgap of AlN and GaN, III-N HBTs are expected to have higher power handling capability, higher breakdown voltage and high-temperature-operation capability than III-V HBTs. A number of *npn* AlGaN/GaN HBTs have been demonstrated with good current gain and high breakdown voltage [33, 34, 35, 36, 37]and the capability to operate at 250 C and 300 C [37, 38, 39]. However, only few of the reported *npn* AlGaN/GaN HBTs are capable of achieving high collector current density (J_C) greater than 1 kA/cm^2. This is attributed to the highly resistive *p*-type base layer caused by the high activation energy of magnesium (Mg) dopant. As a result, the measured f_T is 1 GHz and f_{max} is below 1 GHz with 10 dB/decade roll-off on the *npn* AlGaN/GaN HBTs [40].

To reduce the base resistance, *npn* GaN/InGaN HBTs were implemented with a Mg-doped InGaN base layer [41, 42]. The activation energy of Mg in *p*-InGaN (130 eV for $In_{0.06}Ga_{0.94}N$ [43]) is lower than that in *p*-GaN (> 155 eV for GaN [44]) which helps achieve higher free-hole concentration and lower base sheet resistance [45, 43]. The re-growth technique was also used to grow a highly doped *p*-type contact region after the emitter mesa etching step [16, 17]. The re-grown *p*-layer helps reduce the base contact resistance to retain good current gain and collector current drive in regrown *npn* GaN/InGaN HBTs. However, in the view of manufacture, direct-growth HBTs (DG-HBTs) are still preferred for simpler device fabrication steps and lower growth chamber contamination during regrowth process. *Pnp* GaN/InGaN DG-HBTs have been demonstrated with good current gain (86) and high current density (J_C = 7.3 kA/cm^2) [46]. On the other hand, *npn* GaN/InGaN DG-HBTs are less explored because of the inevitable plasma etching damage and associated type conversion on *p*-type base layer during fabrication processes [47].

At Georgia Tech, the research work was focused on the development of device structure and fabrication processes for GaN/InGaN *npn* DG-HBTs. Nitrogen-incorporated plasma-enhanced dry-etching process was developed and optimized to reduce the etching damage during the mesa etching processes. Different *p*-type metal stacks were used to improve the base contact resistance and the stability of GaN/InGaN *npn* DG-HBTs. The impact of indium content in the base layer was studied to determine the optimal layer structure for GaN/InGaN DG-HBTs. The burn-in effect was also investigated to reduce the hydrogen passivation in *p*-InGaN base layer. The fabricated GaN/InGaN *npn* DG-HBTs grown on free-standing GaN (FS-GaN) substrates

demonstrated high h_{fe} > 110, high current density (J_C) > 141 kA/cm^2 and high power density (P_{dc}) > 3 MW/cm^2. With Pd-based *p*-type contacts, current gain h_{fe} >80, J_C > 93 kA/cm^2 and P_{dc} > 1.3 MW/cm^2 were also achieved on GaN/InGaN *npn* DG-HBTs grown on sapphire substrates. The S-parameter measurement on fabricated GaN/InGaN *npn* DG-HBTs showed f_T > 8 GHz and f_{max} > 1.8 GHz. To our best knowledge, the measured results demonstrated the highest current gain, current density and cut-off frequency for GaN/InGaN *npn* DG-HBTs to date.

1.4 III-N heterojunction field-effect transistors

Field-effect transistors, such as metal-semiconductor field-effect transistors (MESFETs) and junction field-effect transistors (JFETs), have also been a focused research topic for relatively simpler fabrication processes than HBTs. III-V MESFETs [48] and JFETs [49] have been demonstrated with f_T > 100 GHz and 45 GHz, respectively. To achieve better device linearity, a delta-doped channel with a wide bandgap barrier layer is preferred. Therefore, heterojunction field-effect transistors (HFETs) or high-electron-mobility transistors (HEMTs) were implemented. III-V HFETs, such as InGaAs / InAlAs HFETs, have been demonstrated with f_T > 688 GHz and f_{max} > 800 GHz [50]. Many MMICs based on III-V HFET technologies have been commercialized for wireless communication applications. However, the breakdown voltages of III-V MESFETs and HFETs are limited by the small bandgap of III-V semiconductors. For high-voltage applications, SiC MESFETs also have been demonstrated with breakdown voltage >172 V [51]. However, the operation frequency and current drive is much lower than III-V MESFETs and HFETs due to lower carrier saturation velocity in SiC.

On the other hand, III-N HFETs are expected to achieve comparable operation frequency to III-V HFETs with higher operation voltage because of the high carrier velocity and wide bandgap of III-N materials. The strong spontaneous and piezoelectric-polarization effects in III-N materials also enable the formation of two-dimensional electron gas (2DEG) at AlGaN/GaN and InAlN/GaN hetero-interface [52]. In 2DEG, a high sheet carrier concentration (> 1E12 cm^{-2}) with high electron velocity (2.5×10^7 cm/s) can be achieved simultaneously without intentional doping [53]. Therefore, III-N HFETs are expected to be one of the promising devices for the next-generation microwave and power electronics.

Typical III-N HFET structure are gallium-polar (Ga-polar) structure grown on (0, 0, 0, 1) axis. To date, Ga-polar AlGaN/GaN HFETs grown on SiC substrate can achieve the $I_{D,max}$ = 1.2 A/mm, f_T of 70 GHz and f_{max} of 300 GHz [54]. AlGaN/GaN HFETs grown on silicon substrate can achieve the $I_{D,max}$ = 800 mA/mm, f_T of 100 GHz and f_{max} of 206 GHz because of high defect density caused by larger lattice mismatch [55]. Multiple-heterojunction structure have also been demonstrated to achieve f_T and f_{max} of 310 GHz and 364 GHz, respectively [56]. A high output power density in excess of 10 W/mm at 40 GHz [57] and more than 2 W/mm at 80.5 GHz [58] were achieved. Extremely high output power (P_{out}) of 500 W was also demonstrated at L-band [59].

Nitrogen-polar (N-polar) III-N heterojunction can also be grown in (0, 0, 0, -1) axis. N-polar heterostructure offers a natural back-barrier and better electron confinement for than Ga-polar AlGaN/GaN HFETs. N-polar GaN/AlGaN HFETs have been demonstrated with 800 mA/mm, f_T = 18 GHz and f_{max} = 44 GHz [60]. With regrown InN contact layers, lower contact resistance can be achieved [61]. However, compared to Ga-

polar AlGaN/GaN HFETs, lacking of the wide-bandgap barrier layer under gate electrode, a larger gate leakage current is expected. The reversed layer structure also causes lower transconductance because of the larger spacing between gate electrode and 2DEG channel. Therefore, Ga-polar III-N HFETs are still preferred. To increase current drive in Ga-polar HFETs, AlN/GaN HFETs were implemented for the theoretical largest polarization of AlN layer. AlN/GaN HFETs are reported to achieve $I_{D,max}$ = 2.03 A/mm with f_T = 59 GHz and f_{max} = 102 GHz [62]. However, because of the large lattice mismatch between AlN and GaN, the critical thickness of AlN layer is limited at 3~4 nm for AlN/GaN heterojunction. High gate tunneling leakage current becomes a serious issue with such ultrathin barrier heterostructure. The high strain in AlN layer also leads to device instability and short life time for AlN/GaN devices.

To solve the issue caused by lattice mismatch and to enhance the device performance, AlGaN/AlN/GaN HFETs and lattice-matched (LM) InAlN/GaN HFETs are proposed. By inserting a thin AlN binary barrier layer in AlGaN/GaN structure, higher current drive can still be achieved without the issues in AlN/GaN heterojunction structure. As a result, AlGaN/AlN/GaN has become the typical III-N HFETs structure to date. On the other hand, lattice-matched (LM) $In_{0.17}Al_{0.83}N$ can be grown on GaN buffer layer to achieve stress-free InAlN/GaN heterostructure. Compared to AlGaN/GaN heterostructure, InAlN/GaN HFETs also provides higher charge density for higher current drive and cut-off frequency. To date, the reported InAlN/GaN HFETs on SiC substrate can achieve the $I_{D,max}$ = 2 A/mm, f_T of 210 GHz [63]. The InAlN/GaN HFETs grown on silicon substrates can achieve the $I_{D,max}$ = 1.5 A/mm, f_T of 143 GHz and f_{max} of 146 GHz [64].

However, high contact resistance of III-N HFETs is commonly observed due to the wide bandgap of III-N barrier layer. Achievable drain current and cut-off frequency f_{max} are significantly limited by contact resistance. Higher noise is also observed in microwave III-N HFETs. Therefore, selective regrown n^+ layer [65, 19] and ion implantation techniques [66] have been demonstrated to reduce contact resistance of III-N HFETs. With a high doping level in the contact region, non-alloy contact are achievable [61]. However, in the view of process complexity and cost, direct ohmic contact formation is still preferred. Ti/Al/Ti/Au and Ti/Al/Ni/Au are now commonly used for III-N HFETs. Different annealing conditions have been tested for lower contact resistance. However, the achievable specific contact resistance is still > 1E-5 Ω-cm^2 and a high-temperature post-deposition annealing is required.

In addition, most of the reported III-N HFETs have normally-on (depletion-mode or D-mode) characteristics with threshold voltage of -3 to -6 V [67, 68, 69]. In mixed-signal integrated circuits and monolithically integrated circuits, GaN MMICs are interested research topics. To control the threshold voltage of III-N HFETs, several techniques, such as fluorine-treated HFETs [70], *p*-type III-N gate [71, 72] and tunnel junction HFETs [73], have been demonstrated. However, these approaches may have issues in ion-implantation damage and poor threshold voltage control across the sample. On the other hand, the recessed-gate structure is considered advantageous over those approaches for its simplicity and the ability to achieve the desired threshold voltage with higher transconductance. However, recess depth control and etching damage are challenging for dry-etching techniques. Photo-electrochemical wet etching techniques with electrodes [12] and without electrodes [13, 14] also suffer from non-uniform etching

that result in rough etched surface or threshold voltage uniformity issues. Therefore, a new etching technique is required for recessed-gate III-N HFETs to achieve low etching damage and uniform recess depth.

Recent study on III-N HFETs also revealed the influence of surface states on switching performance and device stability of III-N HFETs. The surface states capture electron to form a "virtual gate" which depletes the 2DEG channel when III-N HFETs are switched from the off-state to the on-state. Significant current reduction (current collapse) and gate-lag behavior were observed on III-N HFETs. To passivate surface states, dielectric passivation using PECVD-grown SiN, ALD-grown AlN [24] and HfAlO [25] were reported and showed advantages in suppression of gate-lag and current collapse. Nevertheless, the abrupt heterogeneous interface between the dielectric layer and III-N surface may still contains a high density of interface states. To reduce the density of states, a high-quality native oxide formed on the III-N surface before the dielectric deposition is desired. Surface oxidation techniques on III-nitride materials, such as rapid-thermal-oxidation [26], chemical oxidation [27], and UV-Ozone oxidation [28] have also been demonstrated to grow a thin native oxide layer for surface passivation. Plasma treatment using oxygen plasma [74] or N_2O plasma [10] in plasma-enhanced asher or CVD tools is another effective approach to grow a thin layer of oxide on III-N materials. The previous studies show that the plasma surface treatment helps remove carbon contamination and has beneficial effect on the quality of the dielectric/III-N interface. However, other studies also indicate that deep levels can be created in the AlGaN barrier layer or near the AlGaN/GaN interface due to plasma damage [10, 11]. Therefore, a

damage-free plasma surface treatment is required to passivate the surface states without the undesired damage to III-N HFETs.

At Georgia Tech, a novel in-situ doped contact process was developed to reduce the contact resistance for III-N HFETs without using ion-implantation and regrowth techniques. New Si/Al/Ti/Au metal stacks can achieve 50 % lower specific contact resistance from 8E-6 Ω-cm^2 to 4E-6 Ω-cm^2 with reduced post-deposition annealing temperature from 750 C to 650 C.

With improved ohmic contacts, recessed-gate AlGaN/AlN/GaN HFETs were developed using a new electrode-less wet etching technique. Using AlN layer as the etch-stop layer, a smooth etched surface and potentially uniform device threshold voltage control in III-N HFETs were achieved. The fabricated HFETs show that the threshold voltage can be shifted from -6 V to 0.06 V after wet etching. The standard deviation of V_{th} is < 0.17 V from 60 fabricated recessed-gate HFETs. The transconductance is also increased from 86 mS/mm to 116 mS/mm before and after the recessed-gate etching, respectively. High current drive (420 mA/mm), high breakdown voltage (> 1.2 kV) and low specific on-resistance (6.6 mΩ-cm^2) suggest that the electrode-less wet etching can achieve precise control of threshold voltage with good device performance for E/D-mode III-N HFETs.

A novel remote-oxygen-plasma treatment in a plasma-enhanced atomic-layer deposition (PE-ALD) system was developed to passivate III-N surface without plasma damage. After the plasma treatment, the threshold voltage of recessed-gate AlGaN/AlN/GaN HFETs was shifted 0.25 V toward positive. A two-orders-of-magnitude reduction of the drain leakage current was observed due to the surface native oxide layer.

The capacitance-voltage characteristics of gate diodes showed indistinguishable hysteresis. Improved gate-lag and lowered dynamic on-resistance were observed in the fabricated AlGaN/AlN/GaN HFETs after the oxygen plasma treatment. The results indicate that the oxygen plasma treatment using a PE-ALD system is a promising approach to improve the device switching performance in III-N HFETs.

LM InAlN/AlN/GaN HFETs grown on SiC substrates were also fabricated with a tri-layer e-beam lithography using PMMA/MMA resist. The InAlN/AlN/GaN HFETs with 150nm T-gate demonstrated a maximum transconductance ($g_{m,max}$) of 250 mS/mm at V_{DS} = 3 V and V_{GS} = -4.3 V. The $I_{D,max}$ reached 1.4A/mm at V_{GS} = 1 V and V_{DS} = 10 V. The on-resistance (R_{on}) of 2.24 Ω·mm was measured. For a 2 × 50-μm-wide InAlN/AlN/GaN HFET, f_T of 80 GHz and f_{max} of 106 GHz was measured at V_{GS} = -5 V and V_{DS} = 5 V. The product of cut-off frequency and gate length ($f_T \times L_G$) is 12GHz-μm, which is among the best reported data for InAlN/GaN devices to date.

1.5 III-N metal-insulator-semiconductor field-effect transistors

Although III-N HFETs demonstrate very promising results regarding current drive and breakdown voltage, III-N HFETs still suffers from limited gate voltage swing and higher gate leakage current. The problem can be eased by inserting a gate insulator to form metal-insulator-semiconductor field-effect transistors (MISFETs.) Different gate insulators have been reported on III-N MISFETs, such as SiO_2 [75, 76], Si_3N_4 [77], HfO_2 [78, 79], ZrO_2 [79], MgO [80], Sc_2O_3 [80], TiO_2 [81], ZnO [82]and Al_2O_3 [83, 84] deposited by metal-organic chemical-vapor deposition (MOCVD), plasma-enhanced chemical-vapor deposition (PECVD) and atomic-layer deposition (ALD). Among them,

Al_2O_3 film deposited by ALD technique is one of the most promising approaches for MISFETs because Al_2O_3 has higher dielectric constant (k) than SiO_2 and Si_3N_4 and larger bandgap and thermal stability than other high-k dielectrics such as ZrO_2 and HfO_2. ALD technique also provides uniform deposition and precise thickness control than other deposition techniques. However, previous studies indicated that the ALD deposition recipe and the post-deposition annealing condition have significant impact on the performance of III-N MISFETs with Al_2O_3 gate insulator, especially for gate leakage current and hysteresis [29, 85]. Therefore, an optimized ALD Al_2O_3 deposition recipe is desired for III-N MISFETs.

In addition, the gate dielectric deposition process may introduce high density of interface traps at the insulator-semiconductor interface in III-N MISFETs. To improved device performance and reliability for MISFETs, an understanding of the traps arising from different processing steps becomes critical for further device fabrication optimization. Several studies using deep-level transient spectroscopy (DLTS) have been performed to study traps in III-N Schottky diodes [86][87][88]. Drain current transient and dynamic on-resistance measurements have also been used to characterize the traps in III-N HFETs [89, 90]. These techniques help identify the origins of traps and trap energy levels. Through these studies, one can correlate the traps to device performance of III-N devices.

At Georgia Tech, a study on ALD deposition recipe was conducted by exploring six variables that are relevant to the ALD Al_2O_3 gate dielectrics in III-N MISFETs using a fractional factorial design approach. The most significant variables and interactions were studied for threshold voltage shifting (ΔV_{th}), gate-to-source (GS) diode leakage (I_G)

and *I-V* hysteresis ($\Delta V_{hysteresis}$). Based on the results, an optimal processing condition was obtained to fabricated normally-on AlGaN/AlN/GaN MISFETs with ΔV_{th} < 5 V, GS diode leakage < 1 pA/mm and *I-V* hysteresis < 0.5 V.

With the optimal ALD Al_2O_3 deposition conditions, a comparison study was then performed on recessed-gate AlGaN/AlN/GaN MISFETs with and without the remote-oxygen-plasma treatment. The remote-oxygen-plasma treatment helps reduce the drain leakage current from 100 to 1 pA/mm on the fabricated MISFETs when V_{GS} < -0.5 V. As a result, 2.2×10^{11} on-off ratio is achieved on recessed-gate MISFETs with the use of oxygen-plasma treatment, which is three-orders-magnitude higher than the reported value of 10^8 on D-mode MIS-HEMTs [91] and recessed-gate MIS-HEMT [92]. The sub-threshold slope (*S*) of MISFETs is < 86 mV/dec, suggesting interface trap are reduced by the remote-oxygen-plasma treatment.

The frequency-dependent and light-illumination *C-V* measurements both suggested that lower trap density can be achieved by the oxygen-plasma treatment. Drain current transient measurement was carried out on recessed-gate HFETs and MISFETs to study the trap characteristics. Six common traps were identified in HFETs and MISFETs while an additional trap was presented in the MISFETs which could be related to dielectric-related traps. The results showed that the density of traps with τ of greater than 2 s are not reduced by the oxygen plasma treatment. However, the density of traps with τ < 400 ms can be effectively reduced 30 ~ 70 % by the plasma treatment on HFETs and MISFETs. The study not only showed that the plasma treatment is also beneficial to MISFETs but also help to identify the possible source and characteristics of traps in III-N HFETs and MISFETs.

1.6 The scope of the dissertation

The purpose of this dissertation is to develop the fabrication processes, to characterize the device performance and to investigate the issues for III-N transistors. The III-N materials properties, the current development status, and technical challenges for III-N transistors, including III-N HBTs, HFETs and MISFETs, have been introduced in this chapter.

Chapter 2 describes the fabrication process development and device characterization of GaN/InGaN *npn* DG-HBTs grown on *c*-plane FS-GaN and sapphire substrates at Georgia Tech. The study on base indium content and different substrates will be discussed. The burn-in effect of GaN/InGaN *npn* DG-HBTs is also included. The state-of-the-art d.c. and microwave performance of GaN/InGaN *npn* DG-HBTs will be presented and compared to other reported results in this chapter.

In Chapter 3, the software simulation, fabrication processes and device performance for III-N HFETs, including AlGaN/AlN/GaN HFETs and InAlN/AlN/GaN HFETs will be discussed. The influence of epitaxy layer structures, recessed-gate structure and source-field plate will be discussed using the simulation software (Synopsys Sentaurus.) The influence of a novel electrode-less wet etching will be presented for recessed-gate AlGaN/GaN HFETs fabrication. The improvement in gate-lag and dynamic on-resistance after the remote-oxygen-plasma treatment will also be shown. The measured d.c and microwave performance of InAlN/AlN/GaN HFETs will also be presented in this chapter.

AlGaN/AlN/GaN MISFETs will be discussed in Chapter 4. The influence of the ALD deposition process variables is studied on normally-on AlGaN/AlN/GaN MISFETs

using a fractional factorial design of experiment (2^{6-2} DOE). The device performance of normally-off recessed-gate AlGaN/AlN/GaN MISFETs with and without plasma treatment will be presented. The comparison study on *C-V* measurements and the drain current transient measurement for recessed-gate HFETs and MISFETs will be included to study the influence of plasma treatment and the trap characteristics in recessed-gate AlGaN/AlN/GaN HFETs and MISFETs.

Finally, a summary of the completed work and the discussion of possible schemes toward better devices performance for III-N transistors will be discussed in Chapter 5 in the end of this dissertation.

CHAPTER 2

DEVELOPMENT OF GAN/INGAN HETEROJUNCTION BIPOLAR TRANSISTORS

2.1 Introduction

III-Nitride (III-N) heterojunction bipolar transistors (HBTs) have many inherent advantages over III-N field-effect transistors (FETs) including normally-off characteristics, high-power handling capability and vertical current conduction. Many III-N HBTs have been demonstrated with very promising results in the past few years. However, *npn* GaN/InGaN direct-growth HBTs (DG-HBTs) are less explored due to tremendous technical challenges in material growth and fabrication processes. In this chapter, the current development and achievement of *npn* GaN/InGaN DG-HBTs at Georgia Tech will be discussed.

In this study, we focus on the development of fabrication processes to improve the device performance and stability. A nitrogen-incorporated dry-etching process was developed to overcome the issues of etching-induced damage for GaN/InGaN DG-HBTs. A study on different *p*-type contact metals was also conducted to improve the base resistance and device stability. We also studied different indium content in the base layer for better device performance and base recombination current. An $In_{0.03}Ga_{0.97}N$ base layer was chosen for achieving lower defect density and reduced bulk recombination current in GaN/InGaN DG-HBTs. To reduce hydrogen passivation in *p*-InGaN layer, the burn-in effect in DG-HBTs was also investigated by a constant current stressing. A comparison study showed that free-standing GaN (FS-GaN) substrates provide better heat dissipation

and lower bulk-related recombination current than sapphire substrates. As a result, the fabricated GaN/$In_{0.03}Ga_{0.97}N$ DG-HBTs on FS-GaN substrates achieve high current gain (h_{fe} > 110), high current density (J_C > 141 kA/cm^2) and high power density (P_{dc} > 3 MW/cm^2). With Pd-based *p*-type contacts, the DG-HBTs grown on sapphire substrates also show h_{fe} > 80, J_C > 93 kA/cm^2 and P_{dc} > 1.3 MW/cm^2. High-temperature operation capability up to 250C is achieved with an increased breakdown voltage (BV_{CEO}) up to 160V for DG-HBTs on FS-GaN substrates. For microwave characteristics, the highest cut-off frequency f_T > 8 GHz and f_{max} > 1.8 GHz are achieved for the DG-HBTs on sapphire substrates. Based on the measured d.c and microwave characteristics, a small-signal model for III-N HBTs is developed to explore the limitation of III-N DG-HBTs. These results represent the state-of-the-art d.c and microwave performance for III-N HBTs reported to date.

2.2 Device fundamentals

Unlike field-effect transistors (FETs) controlled by the majority charge carrier in a horizontal channel (majority-carrier devices), bipolar-junction transistor (BJTs) and heterojunction bipolar transistor (HBTs) are controlled by the vertical minority-carrier distribution in the base layer (minority-carrier devices). Because BJTs and HBTs consist of two back-to-back *pn* homojunctions or heterojunctions, the junctions prevent the current flowing through the transistor. Therefore, BJTs and HBTs have normally-off characteristics.

At forward-active condition, BE junction is forward-biased while BC junction is reverse-biased. The current flow through the BE junction (I_E) and BC junction (I_C) can

then be described by the diffusion current equations of the *pn* junction. As shown in Figure 2, for example, the I_E and I_C of a *npn* bipolar transistor can be expressed as:

$$I_E = I_{En} + I_{Bp} \tag{1}$$

$$I_C \sim I_{Cn} \tag{2}$$

where I_{En} and I_{Cn} are the electron current flowing through the BE and BC junctions, respectively. I_{Bp} is the back-injected hole current from the base to emitter. Because BC junction is reverse biased, the hole injunction from base to collector is neglected. The base current (I_B) can be expressed as the difference between I_C and I_E:

$$I_B = I_E - I_C = (I_{En} - I_{Cn}) + I_{Bp} = I_{Br} + I_{Bp} \tag{3}$$

where I_{Br} represents the change of electron caused by carrier recombination when electron traveling from the emitter side to the collector side.

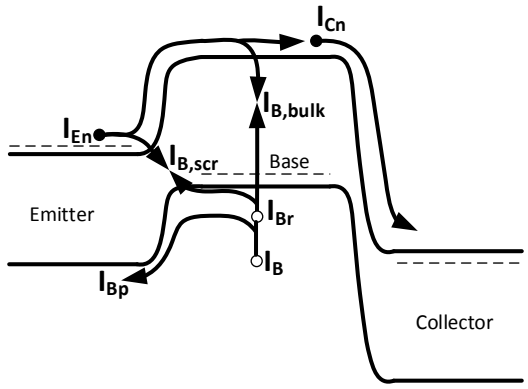

Figure 2. The band diagram of an *npn* bipolar transistor at forward-active condition.

The ratio between I_C and I_B is then defined as the common-emitter d.c. current gain (β) and differential current gain (h_{fe}) :

$$\beta \equiv \frac{I_C}{I_B} = \frac{I_C}{I_{Br} + I_{Bp}} \tag{4}$$

$$h_{fe} \equiv \frac{dI_C}{dI_B} = \frac{dI_C}{d(I_{Br} + I_{Bp})} \tag{5}$$

Based on the current gain definition, the recombination current (I_{Br}) needs to be minimized and the ratio between I_C and I_{Bp} has to be increased to achieve high current gain. Using the diffusion current equation of *pn* junctions, the ratio of I_C and I_{Bp} can be expressed as [93]:

$$\frac{I_C}{I_{Bp}} \sim \frac{D_{nB} X_E N_E}{D_{pE} X_B N_B} \exp\left(\frac{\Delta E_g}{kT}\right) \tag{6}$$

,where D_{nB} and D_{pE} are the electron diffusion coefficient in the base and hole diffusion coefficient in the emitter. X_E and X_B are the thickness of emitter and base, respectively. N_E and N_B are the free-carrier density of emitter and base layer. According to Equation (6), a thin base layer (smaller X_B) with a high carrier mobility (larger D_{nB}) and a heavily doped emitter layer (higher N_E) are preferred to achieve higher current gain.

On the other hand, ΔE_g (= $E_{g,emitter}$ - $E_{g,base}$) is the bandgap difference of the emitter and base layers for a graded BE junction. For an abrupt BE junction, the conduction band energy difference (ΔE_c) replaces the ΔE_g in Equation (6). Therefore, an emitter layer with wider bandgap than base layer is preferred to enhance the ratio of I_C and I_{Bp} for higher current gain. Thus HBTs with wider bandgap emitter are considered superior to BJTs.

For the recombination current, I_{Br} includes four recombination current components caused by different recombination mechanisms at different locations [93]:

$$I_{Br} = I_{B,bulk} + I_{B,scr} + I_{B,surf} + I_{B,cont} \tag{7}$$

,where $I_{B,bulk}$ is the bulk recombination current in the neutral base region. $I_{B,scr}$ is the recombination current in the BE space-charge region. $I_{B,surf}$ is the surface recombination current in the exposed extrinsic base surface region. $I_{B,cont}$ is the interface recombination current at the base contact. The recombination current in the neutral base region ($I_{B,bulk}$) can be expressed as :

$$I_{B,bulk} = \frac{qn_0 X_B A_E}{2\tau_n} \tag{8}$$

,where n_0 is the excess carrier concentration at the emitter-side edge of depletion region for BE junction. n_0 is exponentially dependent on the BE junction voltage ($exp(V_{BE}/kT)$). Therefore, $I_{B,bulk}$ increases with V_{BE} with an ideality factor of 1. τ_n is the effective electron life time in the *p*-type base layer. Thus, to reduce $I_{B,bulk}$, a low-defect thin base layer is required for larger τ_n and smaller X_B. However, the base sheet resistance increases and the achievable current drive degrades when the base layer thickness is reduced. Thus a trade-off exists between the current gain and current drive for bipolar device design.

The BE junction space-charge recombination current ($I_{B,scr}$) is proportional to the width of space-charge region. Therefore, it can be expressed as:

$$I_{B,scr} = I_0 \exp(\frac{qV_{BE}}{2kT}) \tag{9}$$

,where $I_{B,scr}$ increases with V_{BE} but with an ideality factor of 2. I_0 depends on the carrier lifetime in different materials and device designs. Therefore, a low-defect BE junction is required to reduce $I_{B,scr}$.

The surface recombination current ($I_{B,surf}$) is affected by the surface states and recombination centers on the exposed extrinsic base surface. To reduce $I_{B,surf}$, surface passivation using dielectric deposition helps improve current gain for bipolar transistors. $I_{B,cont}$ is the recombination current near the base contacts. However, because the short minority carrier life time in the base layer, $I_{B,cont}$ usually can be neglected if the base contacts are not patterned by self-aligned processes.

Unlike $I_{B,bulk}$ and $I_{B,scr}$ which are proportional to emitter area (A_E), $I_{B,surf}$ and $I_{B,cont}$ are proportional to emitter perimeter (L_E). To investigate the base current components in fabricated devices, normalized current density (J_C/β) at a fixed J_C is plotted against the emitter's perimeter-to-area ratio (L_E/A_E) to extract the perimeter-dependent recombination current ($K_{perimeter}$ in A/cm) and the area-dependent current component (J_{area} in A/cm^2). The relationship of J_C/β, $K_{perimeter}$, and J_{Bulk} can be expressed as follows: [94].

$$\frac{J_C}{\beta} = J_{area} + \frac{L_E}{A_E} K_{perimeter} \tag{10}$$

where β is the d.c. current gain (I_C/I_B), L_E is the emitter perimeter, and A_E is the emitter area. $K_{perimeter}$ is extracted from the linearly-fitted slope of J_C/β data points. $J_{area,}$ is calculated from the intercept of the y-axis (L_E/A_E = 0.) For III-N HBTs without self-align process, $I_{B.cont}$ is neglected and the $K_{perimeter}$ represents the BE junction surface recombination current density ($K_{B,surf} = I_{B,surf} / L_E$). On the other hand, the $J_{area,}$ includes the bulk recombination current density in the neutral base region ($J_{B,bulk} = I_{B,bulk} / A_E$), the recombination current in the space-charge region of BE junction ($J_{B,scr} = I_{B,scr} / A_E$) and the back-injected base current (I_{Bp}).

For GaN/InGaN DG-HBTs, the highly-doped emitter and bandgap difference between GaN emitter and InGaN base help to reduce I_{Bp}. Our previous study on the relationship of β and I_C indicates that J_{area} is dominated by $J_{B,bulk}$ [1]. The EL measurement of GaN/InGaN DG-HBTs also indicates that the recombination process mostly occurs in the InGaN layer [95]. As a result, J_{area} is dominated by $J_{B,bulk}$ and Equation (10) can reveal the amount of $K_{B,surf}$ and the $J_{B,bulk}$.

For microwave performance of BJTs and HBTs, scattering parameters (*S*-parameters) can be directly measured by a vector network analyzer (VNA) or power network analyzer (PNA) with proper calibrations to remove the parasitic capacitance and inductance in the measurement system. With the measured S-parameters, the h_{21} parameter can be obtained by the following equation [96]:

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \tag{11}$$

,where h_{21} represents the ratio of the output current at collector and the input current at base, which is the current gain of the transistor. Thus, the unity current gain frequency (f_T) can be defined at where h_{21} reaches unity. However, h_{21} value may not reach 0dB during the measured frequency range. Therefore, in practice, $|h_{21}|^2$ is plotted in the power gain chart against the measurement frequency. A 20 dB/decade line fitting is drawn on the measured $|h_{21}|^2$ curve to determine f_T .

For bipolar transistors, f_T is determined by the emitter-collector transit time (τ_{ec}):

$$f_T = \frac{1}{2\pi\tau_{ec}} \tag{12}$$

For *npn* bipolar transistors, τ_{ec} is the electron transit time from the emitter contact to the collector contact. Considering the layer structure, τ_{ec} can be separated into four transit time components:

$$\tau_{ec} = \tau_e + \tau_b + \tau_{sc} + \tau_c \tag{13}$$

The first term τ_e is the emitter charging time, which can be further expressed as :

$$\tau_e = \frac{\eta kT}{qI_C}(C_{je} + C_{jc}) \tag{14}$$

,where η is the base current ideality factors. C_{je} and C_{jc} are the junction capacitance of the BE and BC junctions, respectively. It can be seen that a shorter τ_e can be achieve by increasing I_C. Therefore, a high current density is required to achieve higher f_T. On the other hand, C_{je} and C_{jc} can be reduced by shrinking the device area. Therefore, submicron bipolar devices are preferred to better microwave performance. A lower capacitance can also be achieved by lowering the doping levels in devices. However, reducing doping level increases the emitter and collector resistances and degrades device performance.

The second term τ_b is the base transit time for electron to travel through the neutral base region X_B. Therefore, τ_b can be expressed as:

$$\tau_b = \frac{X_B^2}{\nu D_{nB}} \tag{15}$$

,where ν depends on the magnitude of base quasi-electric field caused by bandgap engineering or base doping. Therefore, a thin base layer is desired for a lower τ_b. In addition, a quasi-electric field in the base layer is also preferred to accelerate the carrier transport in the base layer to achieve higher f_T.

The third term τ_{sc} is the BC junction space-charge transit time, which is the time required for electron to drift through the BC depletion region:

$$\tau_{sc} = \frac{X_{dep}}{2v_{sat}} \tag{16}$$

,where X_{dep} is the width of BC junction depletion region and v_{sat} is the electron saturation velocity. Therefore, V_{CB} cannot be high for a smaller X_{dep} to achieve lower τ_{sc}. Some BC junction designs are used to enhance v_{sat} for reducing τ_{sc}.

The last term τ_c is the collector charging time which is the RC charging time caused by emitter and collector resistance:

$$\tau_c = (r_E + r_C)C_{jc} \tag{17}$$

Apparently, lower emitter resistance (r_E) and collector resistance (r_C) are required. A highly-doped sub-collector layer underneath a lightly-doped collector layer is typically used to achieve low r_C and low C_{jc}. A degenerately-doped emitter cap layer is also used to reduce r_E.

The measured *S*-parameters can also be used to calculate the stability factor, maximum available gain (*MAG*), maximum stable gain (*MSG*) and Mason's unilateral gain (*U*) for the maximum oscillation frequency (f_{max}) of the transistor.

For a microwave transistor as a two-port network, the stability determines whether the device oscillates at certain mismatch conditions. Based on the measured S-parameters, the stability factor (*K*) can be calculated by the following equation [96]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{21}S_{12}|^2}{2|S_{12}S_{21}|} \tag{18}$$

If $K > 1$, the transistor is unconditionally stable, which means that the transistor does not oscillate at any matching conditions unless a negative impedance is used. Therefore, the maximum available gain (*MAG*) presents the maximum power gain of the transistor as the following the equation:

$$MAG = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right) \quad \text{when } K>1 \tag{19}$$

However, if $K < 1$ at certain frequencies, the transistor may oscillate at mismatched conditions. Therefore, the maximum power gain is limited to the maximum stable gain (*MSG*) to prevent oscillation:

$$MSG = \frac{|S_{21}|}{|S_{12}|} \quad \text{when } K<1 \tag{20}$$

In addition, the Mason's unilateral gain (U) is also typically used for evaluating transistors. Using Z-parameters derived from S-parameters, U can be calculated by the following equation [97]:

$$U = \frac{|Z_{12} - Z_{21}|^2}{4\left(\mathrm{Re}(Z_{11})\mathrm{Re}(Z_{12}) - \mathrm{Re}(Z_{12})\mathrm{Re}(Z_{21})\right)} \tag{21}$$

Compared to MAG and MSG, U represents the device characteristic and is not affected by the under lossless, reciprocal embedding. Therefore, it is typically used as a figure-of-merit for transistors. In practice, *MAG* (or *MSG*) and U are typically both used to determine the maximum oscillation frequency ($f_{\max}$) where the power gains reach unity. A 20 dB/decade line fitting is also typically drawn to determine f_{max} if power gain does not reach 0dB within the frequency range.

When considering the emitter and collector resistance of a bipolar transistor, the $f_{\max}$ can then be expressed as:

$$f_{\max} = \sqrt{\frac{f_T}{8\pi (RC)_{eff}}} \tag{22}$$

,where $(RC)_{eff}$ is the effective RC time constant which takes all the parasitics into consideration. Assuming that $2\pi f_T << 1/r_e C_{jc}$ and no distributed BC junction RC network is considered, $(RC)_{eff}$ can be expressed as [98, 99]:

$$(RC)_{eff} = r_B C_{jc} + \left[2\pi f_T r_C C_{jc}\right]\left(r_e + \frac{1}{g_m}\right)C_{jc} \tag{23}$$

The equation of f_{max} suggests that a low base resistance (r_B) is important for achieving high f_{max}. Therefore, a low base-contact resistance is also a focused research issue for bipolar transistors.

2.3 Epitaxy layer structure

Based on the basic device fundamentals discussed above, the layer structure of GaN/InGaN HBT in this study follows these design considerations. Wide-bandgap GaN emitter, low-resistance thin InGaN base layer, lightly doped GaN collector and degenerately doped sub-collector are used to achieve better device performance. Single-pass epitaxy growth without re-growth process is also used because of simpler device fabrication processing steps and possible growth chamber contamination.

The GaN/InGaN *npn* DG-HBT layer structures were grown in a Thomas-Swan MOCVD system by Prof. Dupuis group at Georgia Tech. Two layer structures ("Structure-A": GaN/$In_{0.03}Ga_{0.97}N$ DG-HBTs and "Structure-B": GaN/$In_{0.05}Ga_{0.95}N$ DG-HBTs) were chosen for the study on the indium content in the base layer. To compare the impact of different substrates, the same device structure (Sample-A: GaN/$In_{0.03}Ga_{0.97}N$ DG-HBTs) was grown on free-standing GaN (FS-GaN) and sapphire substrates. All the samples have similar epitaxial layer structures except for the indium composition in the base layers and different substrate materials, as shown in Table 2. The electron and hole concentrations were calibrated in test samples prior to actual DG-HBT epitaxial material growth runs. Detailed epitaxial growth techniques are similar to our earlier report [100].

The layer structure growth starts with a 2500-nm unintentionally-doped (UID) GaN buffer layer directly on *c*-plane FS-GaN substrates and sapphire substrates, followed by a 1000-nm highly-doped n^+-GaN sub-collector layer ($n = 3\times10^{18}$ cm^{-3}) and a 500 nm *n*-type GaN collector layer ($n_c = 1\times10^{17}$ cm^{-3}). To mitigate the conduction band discontinuity at the base-collector hetero-junction and the electron blocking effect, the base-collector grading layer is applied. Approximately the same magnesium

concentration ([Mg]~ 4×10^{19} cm^{-3}) and the free-hole concentration (p_B~ 1×10^{18} cm^{-3}) in *p*-InGaN base layer were grown for both designs. After the *p*-InGaN base layer growth, the base-emitter grading layer is also applied to improve the interface and emitter materials quality. The heavily doped emitter layer is incorporated to facilitate low emitter contact resistance, to reduce the Mg-related memory effect, and to enhance the emitter injection efficiency. After the layer growth, an 800C annealing process in a nitrogen environment is used to activate the *p*-type InGaN layer.

Table 2 A summary of layer structure variations of *npn* GaN/InGaN DG-HBTs on sapphire and FS-GaN substrates

Layer	Material		Thickness	Free carrier concentration
	Structure-A	Structure-B		
Emitter cap	GaN	GaN	70nm	$n = 1 \times 10^{19}$ cm^{-3}
Emitter grading	$In_xGa_{1-x}N$ (x = 0–0.03)	$In_xGa_{1-x}N$ (x = 0–0.05)	30nm	$n = 1 \times 10^{19}$ cm^{-3}
Base	$In_xGa_{1-x}N$ (x = 0.03)	$In_xGa_{1-x}N$ (x = 0.05)	100nm	$p = 2 \times 10^{18}$ cm^{-3}
Collector grading	$In_xGa_{1-x}N$ (x = 0.03–0)	$In_xGa_{1-x}N$ (x = 0.05–0)	30nm	$n = 1 \times 10^{18}$ cm^{-3}
Collector	GaN	GaN	500nm	$n = 1 \times 10^{17}$ cm^{-3}
Sub-collector	GaN	GaN	1000nm	$n = 3 \times 10^{18}$ cm^{-3}
Buffer layer	GaN	GaN	2500nm	UID
Sapphire or FS-GaN Substrate				

2.4 Development of fabrication processes

2.4.1 Fabrication process flow

In Figure 3 (a), the device fabrication process starts with a three-step chlorine-based mesa etching in a STS™ inductively coupled plasma (ICP) etching system using e-beam evaporated SiO_2 layers as etching masks. The first mesa etching step is to isolate the GaN/InGaN DG-HBTs by removing the highly conductive sub-collector layer. The following etching process is used to expose the base layer, and the third mesa etching

stops at the sub-collector to expose the contact area for collector contacts. After the ICP etching steps, DG-HBT samples are treated in a diluted KOH/$K_2S_2O_8$ solution under the ultraviolet light illumination to remove the dry-etching-induced damage [101]. Ti/Al/Ti/Au and Ti/Al/Ti/Pt metal stacks are patterned and annealed in a nitrogen environment for the collector and emitter contacts, respectively. Different *p*-type metal stacks, including Ni/Ag/Pt, Ni/Au and Pd/Ni/Au, are patterned and annealed at 500C for 1minute in air to investigate the impact of base metals to device characteristics and reliability. The schematic cross-section of completed DG-HBTs is shown in Figure 3 (b). Figure 4 is the actual scanning-electron microscopy (SEM) picture of a 4×10 μm^2 DG-HBT prior to the passivation steps. Benzocyclobutene (BCB) layer is used to passivate the samples, followed by a via-hole opening dry etching in an ICP etching system. A thick Ti/Au layer is patterned to form the probing pads and co-planar waveguide configuration for microwave characterization.

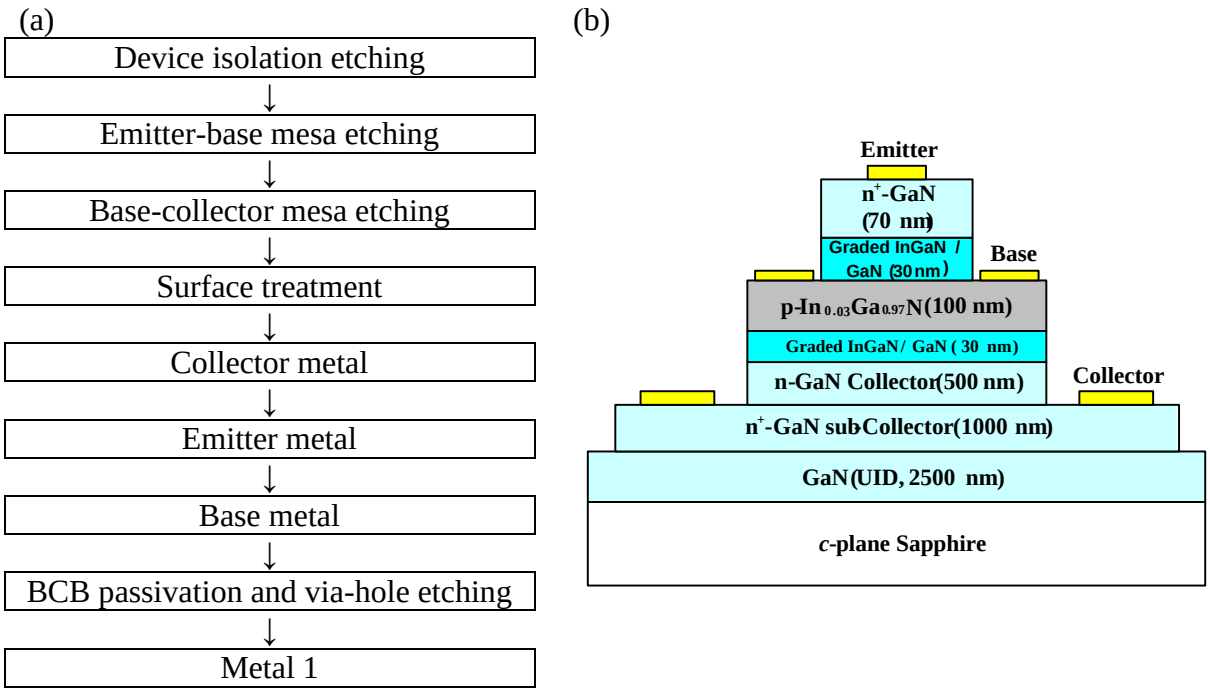

Figure 3. (a) The fabrication process flow and (b) the schematics of the direct-growth GaN/InGaN *npn* DG-HBT before passivation.

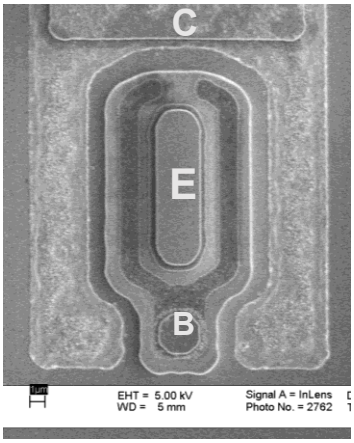

Figure 4. A SEM picture of an A_E = 4×10 μm^2 DG-HBT prior to the device passivation.

2.4.2 Nitrogen-incorporation dry etching process

For *npn* GaN/InGaN DG-HBTs with etched-mesa structure, a low-damaged dry etching process is desired to achieve smooth mesa sidewalls and surfaces as shown in Figure 5 (a). However, rough mesa sidewalls and damaged surfaces are typically observed as show in Figure 5 (b) if the dry etching process is not optimized. To explore an optimal etching recipe, a study on dry etching process with different etching gas was conducted on the etched *p*-InGaN surface of DG-HBT samples.

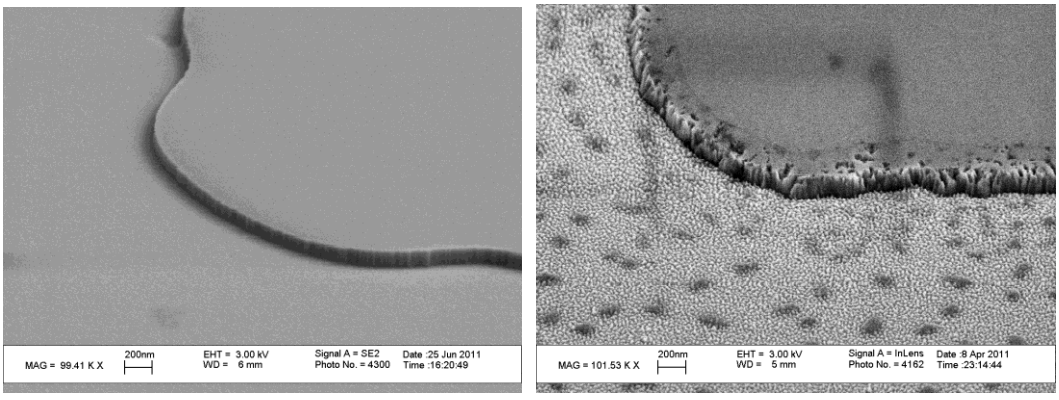

Figure 5. The SEM images on (a) smooth surface and sidewall (b) severely-damaged surfaces and sidewalls.

The etching process study was carried out in a STS™ ICP etching system with a chlorine-based etching gases. Five *npn* DG-HBT samples were cut from the same GaN/$In_{0.05}Ga_{0.95}N$ DG-HBT sapphire wafer (Wafer ID: 1-1391-6) to eliminate the variation caused by the epitaxial growth. The 5 samples were etched by different mixture of etching gases using the same RF plasma power in the STS-ICP system. N_2 and BCl_3 with different flow rates were incorporated in Cl_2-based dry etching process to study different mixture of etching gases during the etching process. The detailed gas flow rate and plasma power and measured etching rate are summarized in Table 3. After the *p*-InGaN layer was exposed by the dry-etching process, Ni/Ag/Au *p*-type contacts were patterned on the etched surface and annealed at 500C for 1 minute in air to form the transmission-line-model (TLM) patterns for I-V measurements.

Table 3 The etching condition applied on DG-HBT samples

Sample	He flow rate (sccm)	Cl_2 flow rate (sccm)	BCl_3 flow rate (sccm)	N_2 flow rate (sccm)	Coil power (W)	Platen power (W)	Etching rate (Å/min)
1	32.5	5	0	0	600	10	<200
2			2.5	0			~500
3			2.5	2			~500
4			0	2			~600
5			0	5			~600

The measured I-V curves of 80 μm-wide TLM pads with 4 μm-spacing on each sample are plotted in Figure 6 and the extracted performance are summarized in Table 4. Sample-1 was etched with a low etching rate (< 200Å/min) when no BCl_3 and N_2 gas is used. The measured TLM *I-V* curve shows very resistive TLM contacts (differential resistance > 3 GΩ at 5 V) and no turn-on characteristics. This results suggest that Cl_2-

based dry etching process requires additional etching species to enhance the etching process on III-N materials [102].

On the other hand, Sample-2 (BCl_3-incorporated etching) and Sample-4 (N_2-incorporated etching) show a higher etching rate than Sample-1. Although Schottky rectifying *I-V* curves are still observed, the TLM *I-V* curves show improved conduction current and differential resistance than Sample-1. A higher conduction current of 18.5 μA is observed with a lower turn-on voltage of 1.1 V on Sample-4 while Sample-2 shows 6.5 μA conduction current and 2.5 V turn-on voltage. A lower differential resistance is also observed on Sample-4 than Sample-2. Therefore, N_2-incorporated dry etching process seems more preferred than BCl_3-incorporated process. This may suggest that the additional N_2 gas may help reduce nitrogen vacancy on the dry-etched III-N surface. This result is similar to the post-etching N_2-plasma treatment which is used to recover the etch-damaged III-N surfaces [103]. However, when increasing the N_2 concentration in the etching gas (Sample-5), the conduction current is reduced by 27 % to 13.5 μA with an increased turn-on voltage of 2 V. In addition, sample-3 which is etched with both BCl_3 and N_2 also shows high resistance (>13 MΩ) and low conduction current (<70 nA). Thus the results indicate excess BCl_3 and N_2 cause surface damage to *p*-InGaN surface which is not preferable for the dry etching process.

Conclusively, the results suggest that a small amount of nitrogen gas incorporated in Cl_2-based dry etching process is beneficial to achieve better etched *p*-InGaN surface for lower turn-on voltage of Schottky contacts, higher conduction current and lower base resistance. However, the Schottky base contacts still limits the base current and the stability of GaN/InGaN DG-HBT is degraded due to the enhanced electromigration of

base contacts. A more reliable *p*-type metal stack with lower contact resistance is required for *npn* GaN/InGaN DG-HBTs.

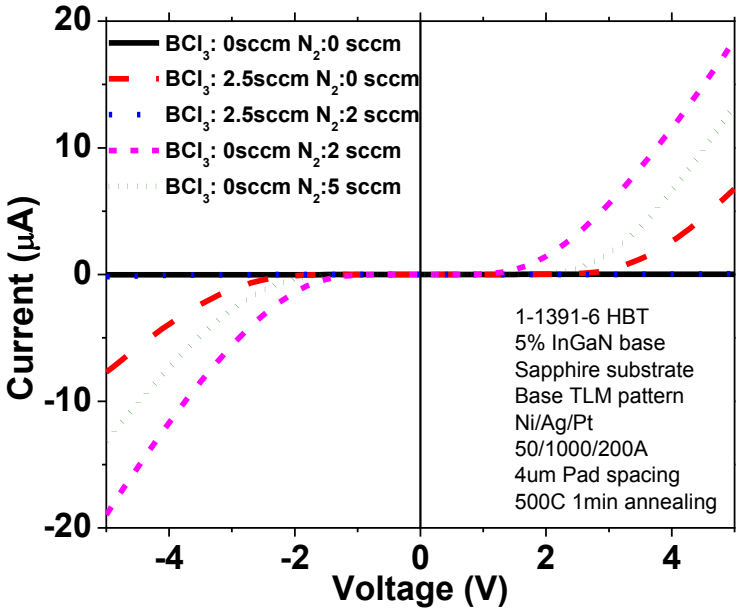

Figure 6. The measured I-V curves of 80 μm-wide *p*-InGaN base TLM pads with 4 μm spacing on DG-HBT samples etched by different recipes (wafer ID: 1-1391-6)

Table 4. A summary of measured *p*-InGaN base TLM I-V performance on DG-HBT samples etched by different recipes (wafer ID: 1-1391-6)

Sample	Turn-on voltage (V)	Conduction current (μA) (at 5V)	Differential resistance (MΩ) (at 5V)
1	>5	0.014	>3000
2	2.5	6.7	0.226
3	>5	0.07	13.7
4	1.1	18.5	0.138
5	2	13.5	0.14

2.4.3 Pd-based *p*-type base metal

Although the nitrogen-incorporated dry etching process improves the *p*-InGaN contacts, the Schottky *p*-type base contacts lead to a quick contact failure and short device life time when being stressed at a high current density. In Figure 7, we observed that a Ni/Ag/Pt (300/500/500Å) *p*-type contact on a GaN/InGaN DG-HBT suffered

significant leakage current after being stressed at high current [1]. The SEM image showed the defect-enhanced catastrophic damage at the base-emitter junction after a high base current stressing. Many vacancies were observed near the edge of Ni/Ag/Pt metal pads. Several spheres and cracks were also generated near the edge of emitter mesa. These may be attributed to the Ag-Ga solid solution formed after base contact annealing [104]. The base current concentrated at several conductive paths and melted the alloyed Ag-Ga layer because of the highly resistive *p*-type contacts. The melted material then re-deposited on the surface to form these spheres and cracks shown in the SEM image.

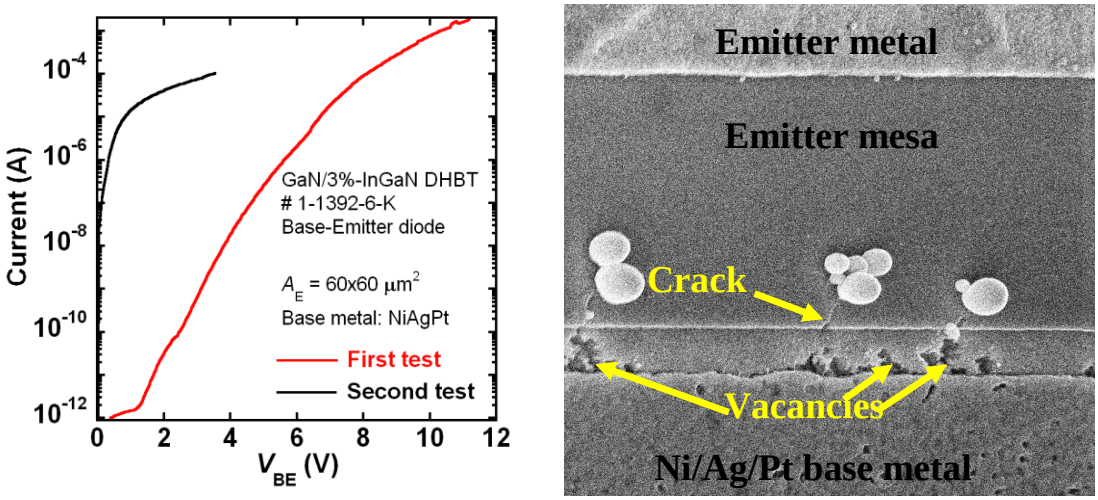

Figure 7. (a)The I-V characteristics of BE junction with Ni/Ag/Pt *p*-type contacts [1] and (b) The SEM images of melted Ni/Ag/Pt *p*-type metal contacts after a high current stressing.

To prevent *p*-type contact failure, Ni/Ag/Pt metal stacks were replaced by Ni/Au stacks (50/50Å). Compared to Ni/Ag/Pt contacts, Ni/Au stacks has less inter-diffusion during the post-deposition annealing. The higher melting temperature of Ni and Au also makes N/Au contacts more robust at high temperature. As a result, the Ni/Au *p*-type contacts showed a more robust contact performance under repeated current stressing without observable contact failure, as shown in Figure 8 (a). However, the common-

emitter family curves of a GaN/InGaN DG-HBT with Ni/Au base contacts showed that the offset voltage (V_{offset}) and the knee voltage (V_{knee}) were increased by 2 V after stressing, as shown in Figure 8 (b). The d.c current gain ($\beta = I_C/I_B$) was also reduced slightly from 20 to 19. Further study indicated that the device degradation is permanent and leads to a leaky BC junction at reverse bias. The leaky BC junction may be attributed to the enhanced electromigration of the metal species in the etched *p*-type base layer at high junction temperature during the constant current stressing. Additional conduction paths are formed between the base metal contact and the underlying extrinsic collector region, which leads to increased offset voltage and device performance degradation.

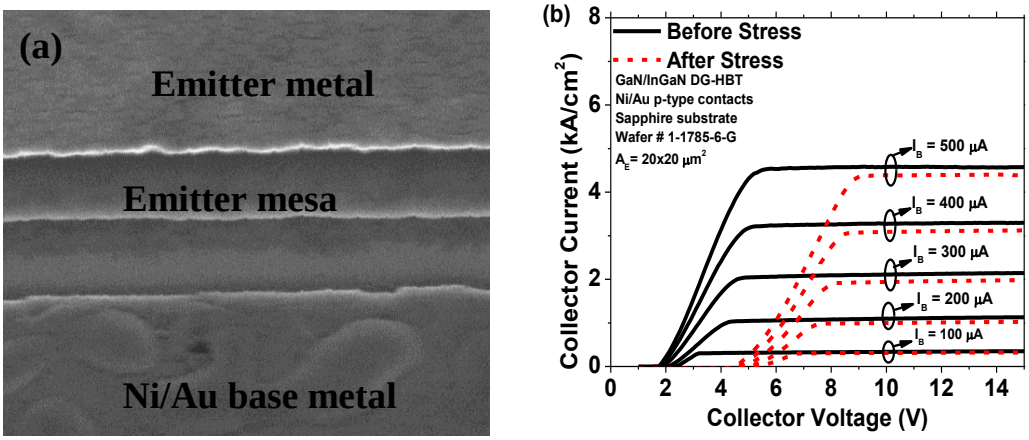

Figure 8. (a) The SEM images of Ni/Au base metal and (b) the common-emitter family curves of a 20 × 20 μm² GaN/InGaN DG-HBT with Ni/Au base contacts before and after high current stressing.

To further improve the stability of *p*-type contacts on GaN/InGaN DG-HBTs, Pd/Ni/Au contacts (100/200/300Å) were tested. Pd has lower diffusion coefficient in InGaN layer than Ni [22] which can prevent the possible electromigration of the metal species in the etched *p*-InGaN base layer. In Figure 9, the I-V characteristics of 80 μm-wide Ni/Au and Pd/Ni/Au TLM patterns with 4, 8, 16, and 32 μm spacing on *p*-type InGaN base layer show that the conduction current is three-times higher at 5V on the Pd/Ni/Au contacts although it is still non-ohmic. In Figure 9 (b), a constant current

stressing test is shown by monitoring the change of the base-emitter voltage (V_{BE}) on two GaN/InGaN DG-HBTs with the same emitter area (A_E = 20 × 20 μm^2) but Ni/Au and Pd/Ni/Au *p*-type base contact schemes. A constant I_B of 100 μA and V_{CE} of 10 V were chosen for the stressing condition in these tests. The V_{BE} of the DG-HBT with Ni/Au contacts became unstable and a large amount of voltage drop was observed when the stress time was greater than 10 min. The reduced V_{BE} of Ni/Au contacts is attributed to the formation of additional leakage path during the current stressing. The device with Pd/Ni/Au *p*-type contact show lower V_{BE} than that of Ni-based contacts which is consistent to the TLM results. The V_{BE} remained relatively stable (ΔV_{BE} < 17 mV) over a 1-hour constant current stressing, indicating no significant contact property changed during the current stressing. As a result, Pd/Ni/Au metal stacks are applied on GaN/InGaN DG-HBTs on sapphire substrates to achieve better device performance and stability.

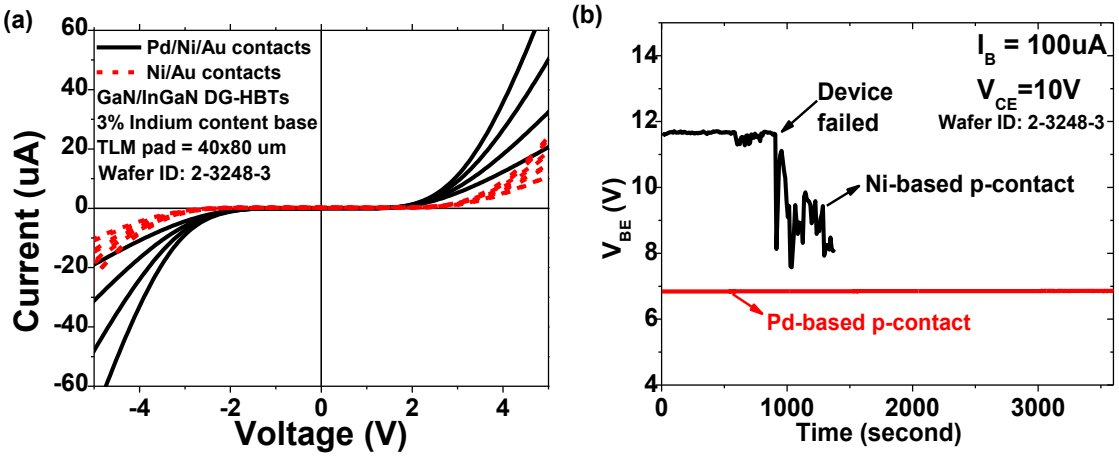

Figure 9. (a) The I-V characteristics of 80 μm-wide Ni/Au and Pd/Ni/Au *p*-type TLM patterns and (b) The time evolution of V_{BE} for GaN/InGaN HBTs under a constant I_B stressing condition in the forward active mode. The DG-HBTs under test have A_E = 20 × 20 μm^2 and I_B = 100 μA at V_{CE} = 10 V.

2.5 D.c. characteristics of GaN/InGaN DG-HBTs

The fabricated GaN/InGaN DG-HBTs were characterized using a Keithley 4200 semiconductor characterization system (SCS-4200) for d.c characteristics at room temperature. Agilent B1505A curve tracer was used to measure the quasi-static characteristics of GaN/InGaN DG-HBTs by pulse measurements.

2.5.1 Study of indium content in base layer

To study the impact of indium content to DG-HBTs, Structure-A and Structure-B DG-HBTs on sapphire substrates (Structure-A for 3% indium content (wafer ID:1-1392-6) and Structure-B for 5% indium content (wafer ID: 1-1391-6)) were fabricated and characterized at room temperature [100, 105, 106]. Figure 10 (a) shows measured Gummel plots of GaN/InGaN DG-HBTs at V_{CB} = 0 V. The emitter area (A_E) is 20 × 20 μm^2 for both devices. The lower voltage of cross-over point for Structure-B (4.3 V vs 4.5 V) indicates the lower base resistance of Structure-B DG-HBTs but the higher cross-over current (230 nA v.s 800 nA) may indicate more recombination current in the base layer. Beyond the cross-over point, the differential current gain ($h_{fe} \equiv dI_C/dI_B$) increases monotonically and reaches 60 at V_{BE} = 13 V for the Structure-A device and 50 at V_{BE} = 11 V for the Structure-B device. Figure 10 (b) shows the common-emitter family curves of both DG-HBTs. Structure-A shows larger maximum J_C (6.25 kA/cm^2) than the Structure-B (5 kA/cm^2) at I_B = 500 μA. The larger knee voltage (V_{knee}) in Structure-A (12 V) than in Structure-B (5V) at I_B = 100 μA indicates that the base resistance is larger in Structure-A.

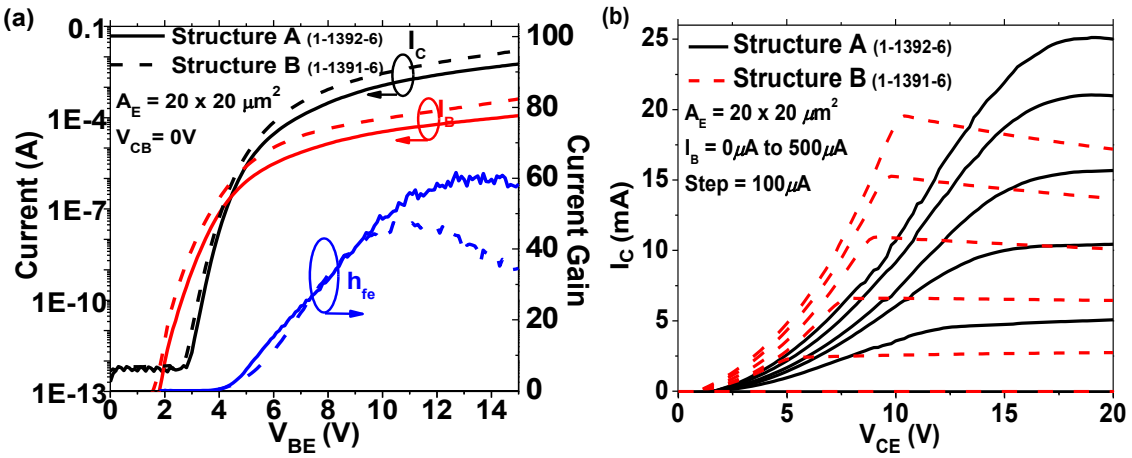

Figure 10. (a)The Gummel plots and (b) the common-emitter characteristics of a Structure-A DG-HBT (solid lines; wafer ID:1-1392-6) and a Structure-B DG-HBT (dashed lines; wafer ID: 1-1391-6) with A_E = 20 × 20 μm^2 grown on sapphire substrates

In Figure 11, J_C/β points measured at J_C = 100 A/cm^2 and 50 A/cm^2 are plotted against the emitter's perimeter-to-area ratio (L_E/A_E) to extract the perimeter-dependent surface recombination current ($K_{B,surf}$) and the area-dependent current component ($J_{B,bulk}$) to investigate the base recombination current for Structure-A and Structure-B DG-HBTs respectively. For a given J_C, the lower $K_{B,surf}$ in Structure-B devices may indicate that the surface recombination velocity decreases as the indium composition increases. The increased $J_{B,bulk}$ in Structure-B DG-HBTs may be attributed to increased growth-related defects such as dislocations and the V-defect formation. These results indicate that a higher indium composition in the base layer helps achieve lower base resistance and reduces the $K_{B,surf}$. These benefits, however, are compromised by the significantly increased $J_{B,bulk,}$ resulting in a lower current gain. Therefore, to achieve lower higher current gain, higher power density and better microwave performance, Structure-A (3% indium content) may be preferred.

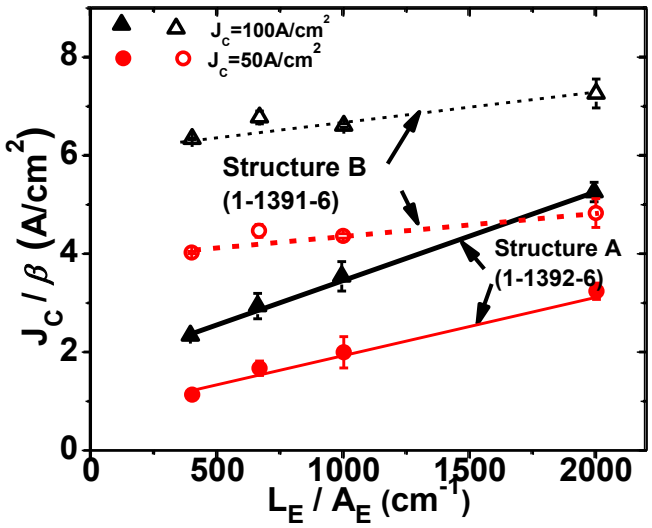

Figure 11. A plot showing J_C/β versus the emitter perimeter-to-area ratio (L_E/A_E) at J_C = 50 and 100 A/cm^2, respectively, for Structure-A (wafer ID: 1-1391-6) and Structure-B (wafer ID: 1-1392-6) DG-HBTs.

Table 5 A summary of J_{Bulk} and $K_{B,surf}$ at different J_C for Structure-A and Structure-B DG-HBTs.

Device Structure	J_C = 100A/cm^2		J_C = 50A/cm^2	
	$J_{B,bulk}$(A/cm^2)	$K_{B,surf}$(A/cm)	$J_{B,bulk}$(A/cm^2)	$K_{B,surf}$(A/cm)
Structure-A (wafer ID: 1-1392-6)	1.79	1.66×10^{-3}	0.8	1.16×10^{-3}
Structure-B (Wafer ID:1-1391-6)	6.36	6.1×10^{-4}	4.2	2.9×10^{-4}

2.5.2 Study of constant current stressing and burn-in effect

To reduce the $J_{B,bulk}$, the burn-in effect in GaN/InGaN DG-HBTs was also studied. As shown in Figure 12, a Structure-B DG-HBT (A_E = 20×20 μm^2) was stressed at constant I_B = 200 μA and V_{CE} =15 V for a period of 50 minutes to explore the time-dependent device performance evolution. It was observed that I_C first increased and then reached a stabilized value of 9.7 mA beyond the stress time > 30 min. At the same time, V_{BE} dropped slightly from 12.4 V to 12 V for stress time > 20 min. After the 50-minute constant-base-current stressing, the peak h_{fe} was increased from 42 to 66 and stayed unchanged afterward for > 1 month. The contact properties for emitter, base, and

collector remained unchanged before and after the burn-in process. This phenomenon is a direct analogy to what has been reported in MOCVD-grown InP/InGaAs or InGaP/GaAs HBTs, known as "the burn-in effect" [107, 108, 109]. It is known that the hydrogen passivation may be significant in MOCVD-grown Mg-doped *p*-type III-N epitaxial layers. Atomic hydrogen forms complexes with Mg in *p*-type III-N materials and a post-growth annealing step needs to be used for the free-hole activation of InGaN:Mg [110, 111]. Similarly, a post-processing current stressing may induce a high junction temperature which is helpful to reduce or eliminate the hydrogen passivation in the *p*-InGaN base layer of DG-HBTs.

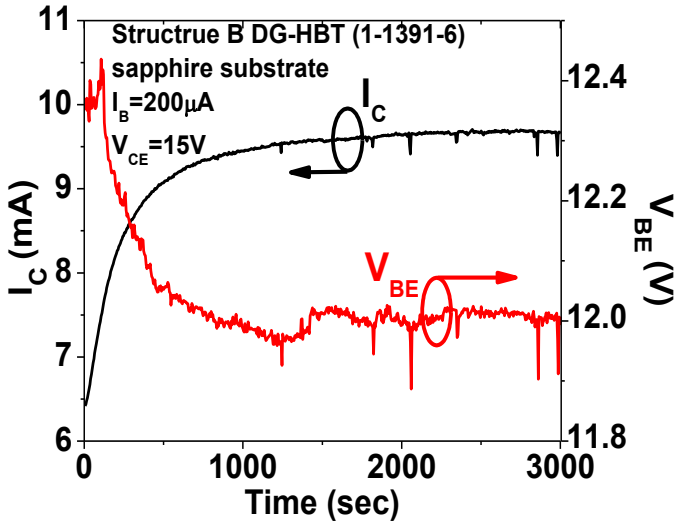

Figure 12. Time-dependent I_C and V_{BE} measure for a Structure-B DG-HBT (wafer ID: 1-1391-6) with A_E = 20 × 20 μm^2 under constant base current stressing (I_B = 200 μA).

The base recombination current components were then extracted from stressed Structure-B GaN/InGaN DG-HBTs and compared with those obtained prior to the device burn-in at J_C = 100A/cm^2, as shown in Figure 13. The results show that $K_{B,surf}$ remains approximately unchanged before and after the current stressing. However, $J_{B,bulk}$ is reduced from 6.2 A/cm^2 to 3.8A/cm^2 after the burn-in. As a result, the reduction in $J_{B,bulk}$

through the device burn-in suggests that the hydrogen passivation in the *p*-type region is alleviated.

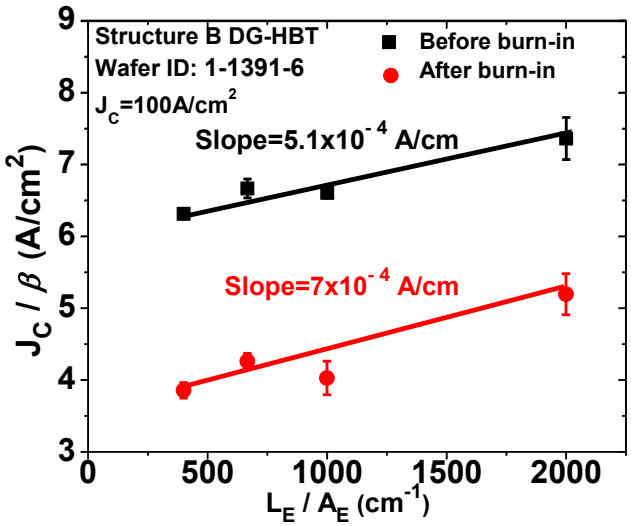

Figure 13. (J_C/β) plotted against (L_E/A_E) for a Structure-B DG-HBT (wafer ID: 1-1391-6) before and after the device burn-in procedure.

Small-signal capacitance-voltage (*C*-*V*) measurements were performed for both BE and BC junctions of Structure-B DG-HBTs before and after the device burn-in. Since the emitter is degenerately doped (2×10^{19} cm^{-3}), the emitter electron concentration is at least one order of magnitude higher than the free-hole concentration in the base. Consequently, the depletion width of the BE junction falls mostly in the base layer. Similarly, the depletion region of the BC junction falls mostly in the lightly-doped collector region. For a one-side abrupt junction, the depletion capacitance can be expressed as [112]:

$$\frac{1}{C^2} = \frac{1}{A^2} \cdot \frac{2}{q\varepsilon_s\varepsilon_0 N}\left(V_{bi} - V\right) \tag{24}$$

where ε_0 is the free-space permittivity. ε_s is the relative permittivity of the lower-doped side of the junction. A is the junction area. V_{bi} is the built-in potential that includes the heterojunction bandgap discontinuity. N is the free carrier concentration of lowly-doped

semiconductor. Therefore, for the BE junction with lowly-doped *p*-type base layer, the free hole concentration in the base layer (p_B) can be determined by the slope (S) of the $1/C^2$ curve for the reverse-biased by:

$$p_B = \frac{1}{A^2} \cdot \frac{2}{q\varepsilon_s\varepsilon_0 S} \tag{25}$$

Likewise, the free-electron concentration of lowly-doped collector (n_C) can be determined from the slope of $1/C^2$ for the BC junction. Figure 14 shows $1/C^2$ curves for the reverse-biased BE junction and the BC junction, respectively, for a Structure-B DG-HBT with emitter are (A_E) = 40×40 μm^2 and collector area (A_C) = 65×100 μm^2. The *C*-*V* measurement is carried out in an Agilent 4284A LCR meter at a frequency of 1 MHz. The slope of $1/C^2$ is extract at 0 to -2V because the slope is reduced at higher reverse bias voltage when the lowly-doped side starts to be fully depleted. Before the burn-in step, p_B is 8.76×10^{17} cm^{-3} and n_C is 1.1×10^{17} cm^{-3}. After the constant base-current stressing, p_B is increased to 1.16×10^{18} cm^{-3}, which corresponds to > 25 % increase in the free hole concentration. On the other hand, the $1/C^2$ curve and n_C for the BC junction remain approximately unchanged, indicating that the measured BC junction remains unchanged after the device burn-in. The extracted V_{bi} for the BE junction is ~ 4.1 V and V_{bi} for the BC junction is 4.3 V. The large V_{bi} is attributed to the Schottky barrier at the base contact. Based on the results, we conclude that the post-processing current stressing method is an effective approach to improve the III-N HBTs' performance by reducing the bulk recombination current and by increasing free-hole concentration in the *p*-InGaN base.

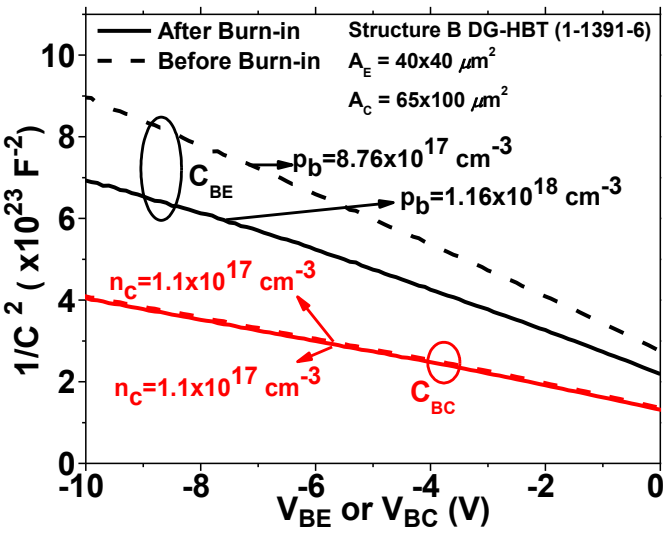

Figure 14. ***1/C²*** **versus applied voltage for the BE and the BC junctions of a Structure-B (wafer ID: 1-1391-6) DG-HBT with** A_E **= 40 × 40 μm² before (dashed lines) and after (solid lines) device burn-in.**

A similar post-fabrication burn-in procedure was also applied on Structure-A DG-HBTs. The device under test has A_E = 20 × 20 μm^2 and the burn-in step was carried out at I_B = 200 μA and V_{CE} = 15 V. Figure 13 shows the Gummel plots and the common-emitter family curves for a Structure-A GaN/InGaN DG-HBT before and after the device burn-in procedure. After the device burn-in, the peak h_{fe} is improved by 75 % from 60 to 105. V_{BE} at the peak current gain is reduced from 13 to 10 V, indicating that the base resistance is reduced with the increased free-hole concentration.

In the common-emitter family curves, it can be seen that, for a given I_B, the collector current drive is greatly improved after the device burn-in. For example, I_C is increased from 5 to 8.4 mA at I_B = 100 μA, which shows> 60% of increase in I_C. The knee voltage (V_{knee}) is reduced from 12 to 10 V at I_B = 100 μA, and the maximum I_C reaches > 26 mA (J_C > 6.5 kA/cm^2) at I_B = 500 μA.

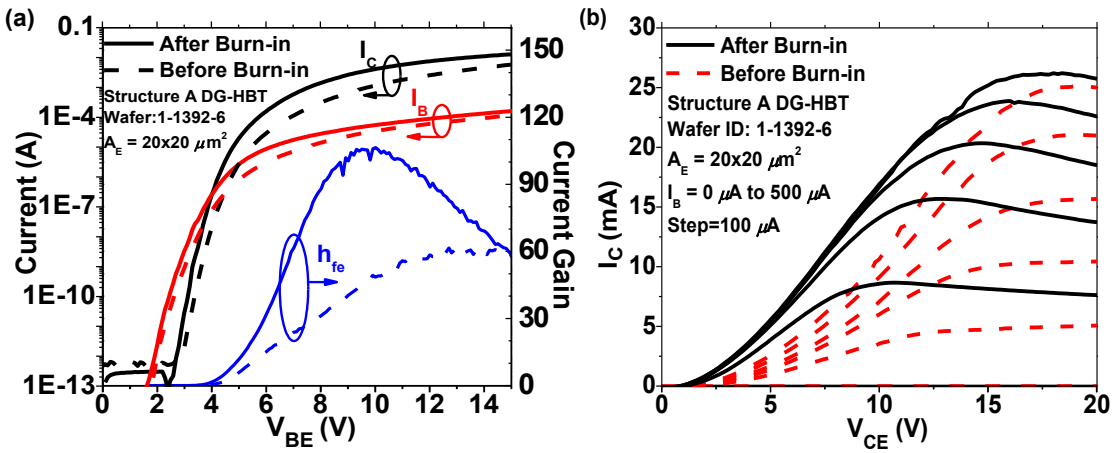

Figure 15. (a) The Gummel plot and (b) the common-emitter family curves of a Structure-A (wafer ID: 1-1392-6) DG-HBT with A_E = 20 × 20 μm² before (dashed lines) and after (solid lines) the device burn-in.

2.5.3 Study of FS-GaN and sapphire substrates

.Compared to sapphire substrates, FS-GaN substrates provide better thermal conductivity and lower defect density caused by lattice mismatch between III-N epitaxial layer and substrate. To investigate the influence of substrates to the performance of DG-HBTs, Structure-A GaN/InGaN DG-HBTs (3% indium content in the base layer) were grown on free-standing GaN (FS-GaN) substrates (wafer ID: 1-1793-6) and sapphire substrates (wafer ID: 1-1785-1) in a Thomas–Swam metalorganic chemical vapour deposition (MOCVD) system [113].

The FS-GaN and sapphire substrate samples were then processed together to reduce the variation caused by fabrication processes. Ni/Au *p*-type contacts were used as base contacts on the two samples. In Figure 16, the measured Gummel plots for GaN/InGaN DG-HBTs (A_E =11.7 μm²) on the FS-GaN and sapphire substrates are shown. In the Gummel plots, I_B and I_C cross over at 0.2 and 0.7 μA for DG-HBT on FS-GaN and sapphire substrates, respectively. The lower cross-over current on FS-GaN substrate suggests a lower base recombination current is achieved. Beyond the cross-over

point, the differential current gain ($h_{fe} = dI_C/dI_B$) reaches maximum values of 110 on FS-GaN substrate and 76 on sapphire substrate at V_{BE} = 11.5 V, respectively. The lower current gain indicates that the base recombination current is higher in the DG-HBTs grown on sapphire substrates. In Figure 16 (b), the DG-HBT on the FS-GaN substrate shows I_C > 15 mA (J_C > 125 kA/cm^2) at I_B = 175 μA and V_{CE} = 10 V. The DG-HBT on sapphire substrate, however, only achieves J_C > 51 kA/cm^2 (I_C = 6 mA) at I_B = 100 μA. The lower operable J_C on the sapphire substrate could be attributed to the increased density of recombination centers and the poor heat conduction of the sapphire substrate.

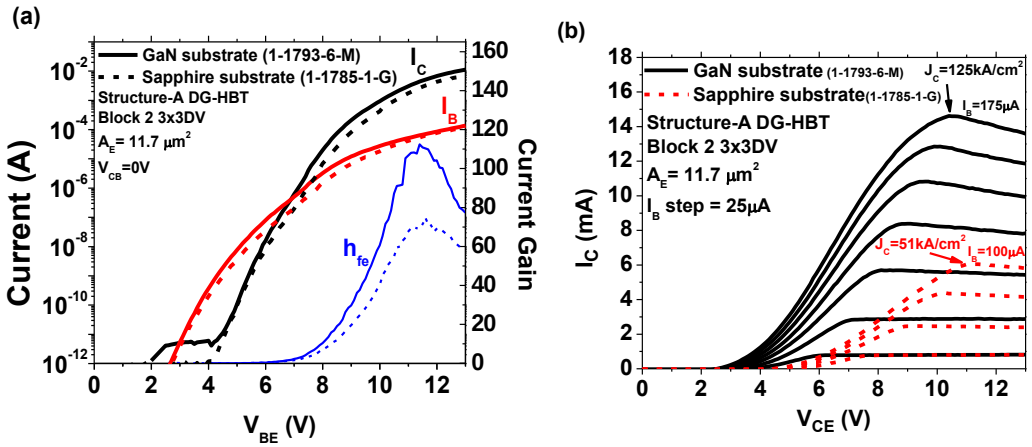

Figure 16. (a)The Gummel plots and (b) common-emitter family curves of GaN/InGaN DG-HBTs with A_E = 3 × 3 μm^2 on FS-GaN substrate (wafer ID: 1-1793-6) and on a sapphire substrate (wafer ID: 1-1785-1) at room temperature.

By plotting (J_C/β) versus (L_E/A_E) for different-sized DG-HBTs on sapphire and FS-GaN substrates at J_C =1000, 500 and 100A/cm^2, the base recombination components can be extracted as shown in Figure 17. The extracted values are summarized in Table 6. It is noticed that the bulk recombination current ($J_{B,bulk}$) is more than 4 times higher for DG-HBTs grown on sapphire substrates than those on FS-GaN substrates. The surface recombination current ($K_{B,surf}$) is also slightly higher on sapphire substrates. The results

indicate that lower dislocation density caused by lattice-matched FS-GaN substrate can significantly improve the base recombination current for better current gain.

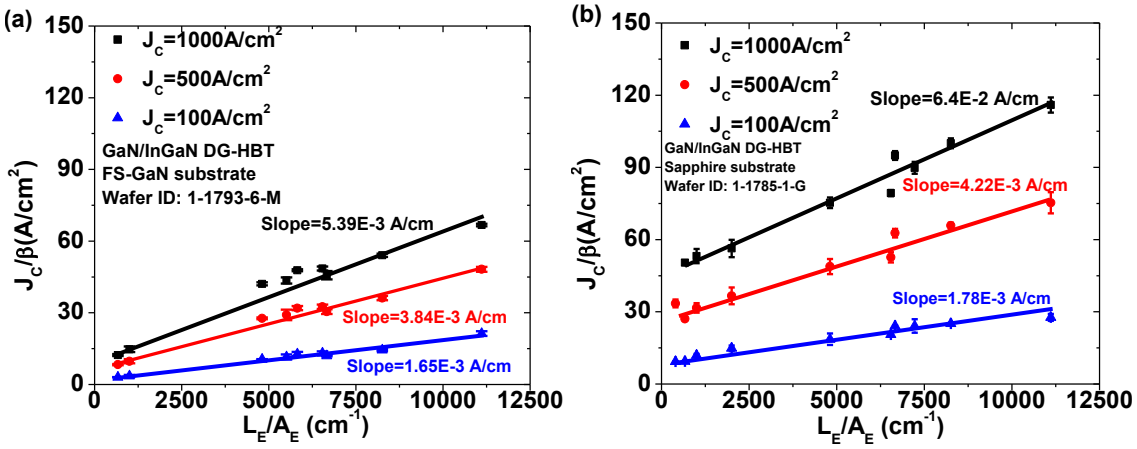

Figure 17. (J_C/β) plotted against (L_E/A_E) for GaN/InGaN DG-HBTs on (a) FS-GaN substrates (wafer ID: 1-1793-6-M) and (b) sapphire substrates (wafer ID: 1-1785-1-G).

Table 6 A summary of $J_{B,bulk}$ and $K_{B,surf}$ at different J_C for GaN/InGaN DG-HBTs on FS-GaN and sapphire substrates.

Device Structure	J_C = 1000A/cm^2		J_C = 500A/cm^2		J_C = 100A/cm^2	
	$J_{B,bulk}$ (A/cm^2)	$K_{B,surf}$ (A/cm)	$J_{B,bulk}$ (A/cm^2)	$K_{B,surf}$ (A/cm)	$J_{B,bulk}$ (A/cm^2)	$K_{B,surf}$ (A/cm)
FS-GaN substrate (1-1793-6-M)	10.47	5.39E-3	6.52	3.84E-3	2.05	1.65E-3
Sapphire substrate (1-1785-1-G)	45.16	6.4E-2	28.18	4.22E-3	9.96	1.78E-3

Compared to DG-HBTs on FS-GaN substrates, DG-HBTs on sapphire substrate also showed a shorter device life time. This indicates that the poor heat conduction of sapphire substrate may result in higher junction temperature and enhances the electromigration of base contacts. To prevent device failure and enhance device performance, Pd/Ni/Au *p*-type contacts was applied on DG-HBTs on sapphire substrates. Further improvement in material growth was also made to reduce the growth defects on sapphire substrate (wafer ID: 2-3248-3).

The measured Gummel plots for GaN/InGaN DG-HBTs (A_E =11.7 μm^2) with Pd/Ni/Au p-type contacts on a sapphire substrate (wafer ID: 2-3248-3) is shown in Figure 18. With the new Pd/Ni/Au contacts, I_B and I_C cross over at V_{BE} = 4 V which is lower than 7V on DG-HBT with Ni/Au contacts. The differential current gain (h_{fe} = dI_C/dI_B) reaches similar maximum values of 76 at V_{BE} = 9 V. The lower cross-over voltage and lower V_{BE} at peak current gain indicate lower base resistance is achieved for DG-HBT with Pd/Ni/Au contacts on the sapphire substrate.

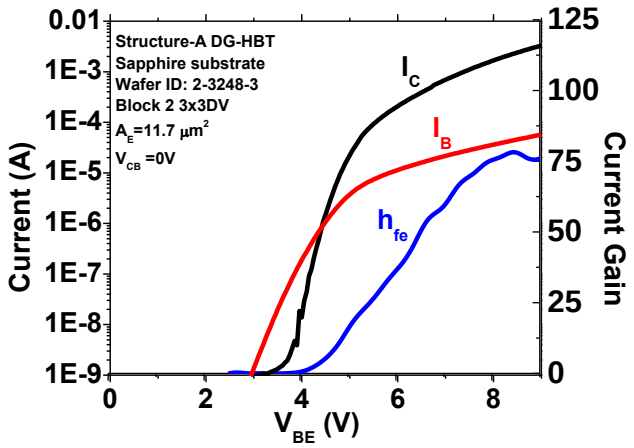

Figure 18 The Gummel plot of GaN/InGaN DG-HBTs with Pd/Ni/Au contacts on a sapphire substrate (wafer ID: 2-3248-3-A) at room temperature.

To explore the maximum achievable current and power density of DG-HBTs, the common-emitter family curves of DG-HBT grown on the FS-GaN and sapphire substrates were measured using an Agilent B1505 curve tracer. A quasi-static measurement setup (1 ms pulse with a repetition rate of 2 Hz) was used to reduce the self-heating during measurement. As shown in Figure 19, a maximum J_C > 141 kA/cm^2 at V_{CE} = 20 V and an ultra-high power density ($P_{d.c}$) of 3.05 MW/cm^2 were achieved on FS-GaN substrates [114]. The DG-HBT with Pd-based *p*-type contacts on the sapphire substrate, however, achieved J_C > 95 kA/cm^2 and $P_{d.c}$ > 1.3MW/cm^2 at I_B = 240 μA due

to lower current gain and poor thermal conductance of the sapphire substrate. Nevertheless, to our best knowledge, the achieved current density (141 kA/cm^2 on FS-GaN and 95 kA/cm^2 on sapphire) and power density (3.05MW/cm^2 on FS-GaN and 1.33MW/cm^2 on sapphire) are the highest values reported for III-N DG-HBTs to date.

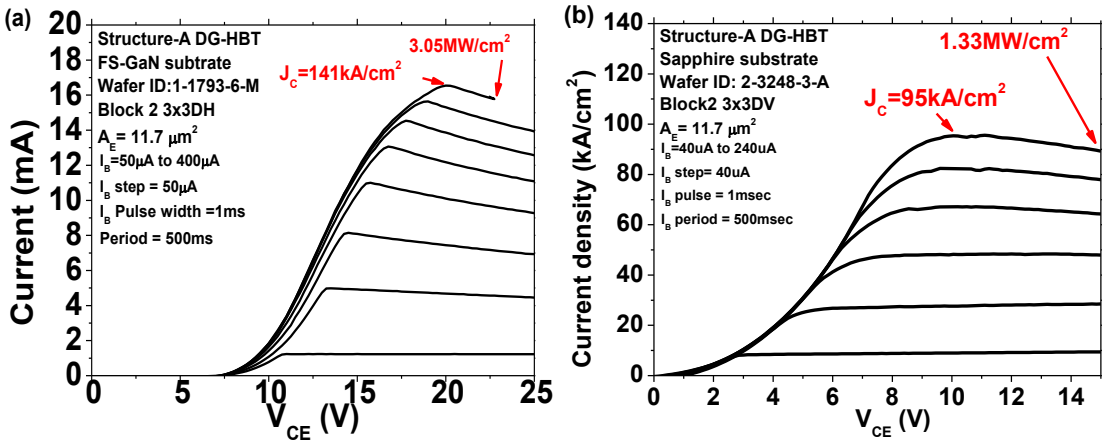

Figure 19. The quasi-static common-emitter family curves of GaN/InGaN DG-HBTs with A_E = 3 × 3 μm^2 on (a) FS-GaN substrate and (b) on a sapphire substrate at room temperature.

As shown in Figure 20, the breakdown voltages (BV_{CEO} and BV_{CBO}) measured on FS-GaN substrate reach >150V which is twice higher than those measured on sapphire substrates (>75V). The higher breakdown voltage on FS-GaN substrate is attributed to the better material quality and lower defect density. As a result, the product of breakdown voltage and current density ($BV_{CEO} \times J_C$) of *npn* GaN/InGaN DG-HBTs on FS-GaN substrates achieves 21 MW/cm^2. The result is greater than 10 times of those achieved on *pnp* AlGaN/GaN HBTs grown on FS-GaN substrates [46] and more than 1.5 times higher than any state-of-the-art HBTs [115, 116, 117].

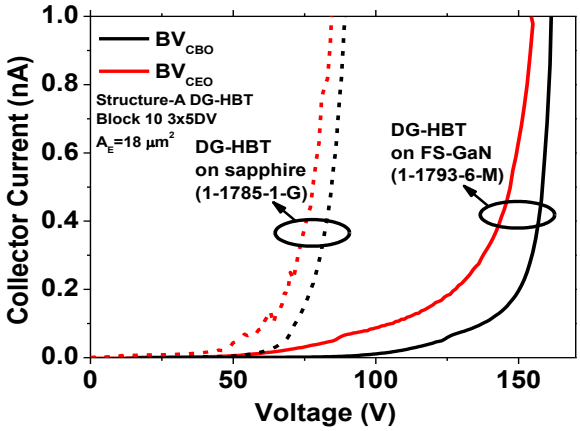

Figure 20. The breakdown voltages of 3×5 μm^2 Structure-A (3% InGaN) DG-HBTs on FS-GaN substrates (wafer ID: 1-1793-6-M) and sapphire substrates (wafer ID: 1-1785-1-G)

In Figure 21, a competitive chart summarizes the reported maximum current density (J_C) versus the current gain (h_{fe}) for III-N HBTs grown on sapphire, SiC and FS-GaN substrates. *Pnp* III-N HBTs are also included in this chart for comparison. In this chart, the GaN/InGaN DG-HBTs fabricated at Georgia Tech show state-of-the-art high current density with high current gain than other III-N HBTs. To our best knowledge, the results are the best device performance of III-N HBTs to date.

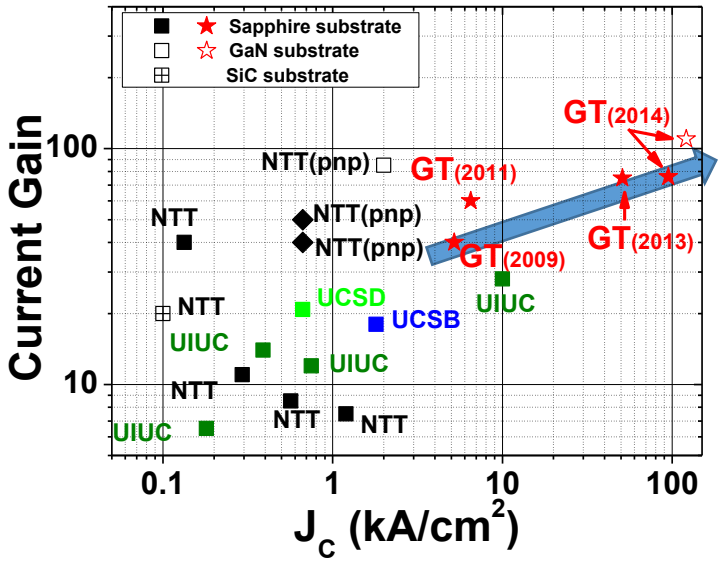

Figure 21. The comparison of maximum current density versus current gain for III-N HBTs on different substrates [17] [37, 38, 118, 106, 114, 119, 35].

2.5.4 Temperature-dependent performance

The *npn* GaN/InGaN DG-HBTs grown on a FS-GaN substrate (wafer ID: 1-1793-6) were also tested on a temperature controlled chuck to study the impact of high temperature to the device performance and the breakdown mechanism. In Figure 22, the Gummel plots and common-emitter family curves of a 40 × 40 μm^2 GaN/InGaN DG-HBT on the FS-GaN substrate at 250C and room temperature (25C) are shown. In the Gummel plots, it is worth to note that the base current is significantly increased at 250 C. For the common-emitter family curves shown in Figure 22(b), the offset voltage is reduced from 0.8 V at 25 C to 0.3 V at 250 C. Similarly, the knee voltage is reduced from 5.2 to 2.75 V at I_B = 500 μA as the temperature increases from 25 C to 250 C. These results indicate that the base resistance is reduced due to higher free-hole concentration caused by enhanced Mg ionization efficiency at 250 C. The maximum differential current gain ($h_{fe} = dI_C/dI_B$) is reduced from 115 to 43 at V_{BE} = 11.2 V when the temperature increases to 250C. The reduced current gain may be attributed to the increased trap-state recombination rate and possibly a lower emitter injection efficiency caused by the higher free-hole concentration at 250 C.

The BV_{CEO} of the device at 25 C and 250 C is shown in the inset of Figure 22 (b). The results show that BV_{CEO} increases from 90 V to 157 V as the temperature increases from 25 C to 250 C. The positive temperature coefficient for BV_{CEO} indicates that the impact ionization process is the major breakdown mechanism for the fabricated GaN/InGaN DG-HBTs grown on a FS-GaN substrate.

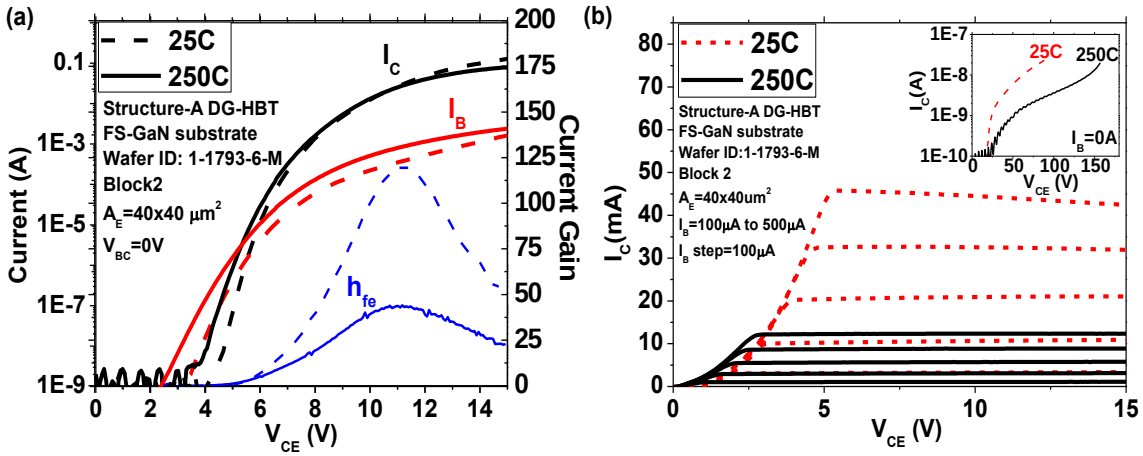

Figure 22. (a)The Gummel plots and (b) the common-emitter family curves of a DG-HBTs with A_E = 40 × 40 μm^2 on a FS-GaN substrate (wafer ID: 1-1793-6-M) at 250 C (solid lines) and 25 C (dashed lines). The breakdown voltage BV_{CEO} is shown in the inset.

For statistical study, five GaN/InGaN DG-HBTs with A_E = 40 × 40 μm^2 were measured from room temperature up to 250 C. The measured maximum current gain (h_{fe}) and the corresponding J_C at maximum h_{fe} are summarized in Table 7. For comparison, the performance of other reported III-N HBTs measured at high temperature are also included in Table 7. The GaN/InGaN DG-HBTs fabricated at Georgia Tech demonstrated a higher h_{fe} up to 250 C than other reported III-N HBTs. The J_C at maximum h_{fe} is also more than 50 % higher than other III-N HBTs at high temperature. The capability of operating at high temperature with higher current gain is attributed to the lower recombination current and more stable metal contacts achieved at Georgia Tech.

Table 7. A summary of h_{fe} and J_C of III-N HBTs at room temperature and high temperature

	Averaged h_{fe} at room tmperature	J_C at peak h_{fe} at room tmperature (kA/cm^2)	Averaged h_{fe} at high temperature	J_C at peak h_{fe} at high temperature (kA/cm^2)	Ref
GT (GaN/InGaN HBT)	113$_{\pm 9.5}$	1.74$_{\pm 0.25}$	42$_{\pm 2.3}$ (at 250C)	1.68$_{\pm 0.29}$	
UCSB (AlGaN/GaN HBT)	20	~1	20 (at 177C)	~1	[37]
UCSD (GaN/InGaN HBT)	20	1.6	13 (at 200C)	0.52	[38]
NTT (AlGaN/GaN HBT)	38	~0.5	30 (at 200C)	~0.5	[39]

2.6 Microwave characteristics of DG-HBTs

With the promising d.c device performance of GaN/InGaN DG-HBTs, devices grown on sapphire substrates were also evaluated the microwave performance of III-N DG-HBTs at Georgia Tech. Although FS-GaN substrates offer better device performance than sapphire substrates, the significant signal loss through the conductive FS-GaN substrates prevents the further microwave characterization.

2.6.1 S-parameter measurement

Before microwave characterization, Structure-A ($In_{0.03}Ga_{0.97}N$ base) DG-HBTs grown on a sapphire substrate (wafer ID: 1-1785-1) were characterized by Keithley semiconductor parameter analyzer at room temperature. To prevent possible device degradation, DG-HBTs were measured at a lower voltage and current density than the bias condition for microwave characterization. In Figure 23, the measured Gummel plot and the common-emitter family curves for the GaN/InGaN DG-HBTs (A_E =5 × 20 μm^2) on the sapphire substrate are shown. In the Gummel plots, the differential current gain ($h_{fe} = dI_C/dI_B$) reaches maximum values of 28 at V_{BE} = 10 V. The lower current gain than the device with A_E =3 × 3 μm^2 suggests that the bulk recombination current dominates the recombination current in DG-HBTs. In Figure 23 (b), the offset voltage (V_{offset}) and the knee voltage (V_{knee}) are smaller than 0.3 V and 0.8 V respectively. The small V_{offset} and V_{knee} suggest that the GaN/InGaN DG-HBT has relatively smaller base resistance than other devices, which is benificial for better microwave performance. This may be attributed to the special design of strip-shaped emitter and small spaciing between base contact and emitter mesa (<0.5 μm.)

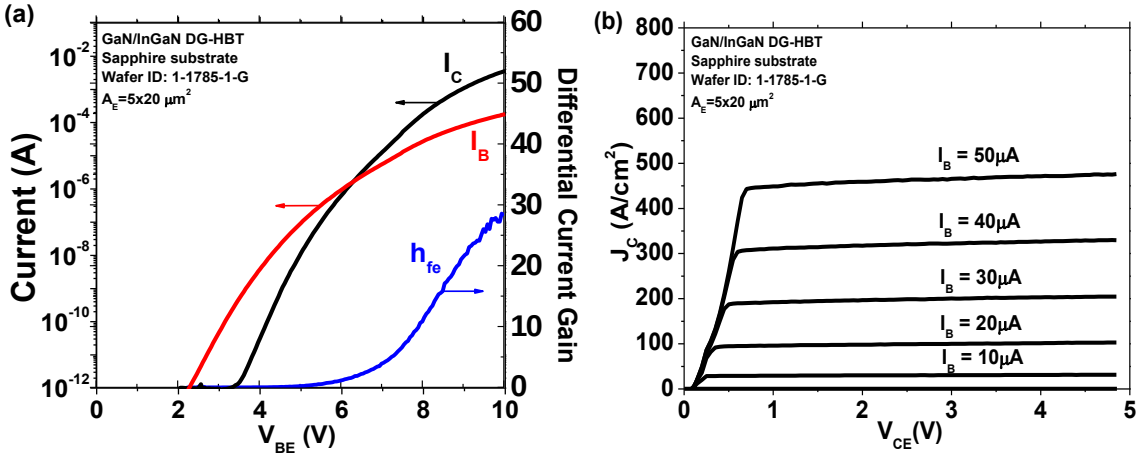

Figure 23. (a)The Gummel plots and (b) the common-emitter family curves of the DG-HBTs with A_E = 5 × 20 μm² on a sapphire substrate (wafer ID: 1-1785-1) at room temperature before microwave characterization.

The microwave performance of Structure-A GaN/$In_{0.03}Ga_{0.97}N$ DG-HBTs on sapphire substrates (wafer ID: 1-1785-1) were then carried out using an Agilent E8364B power network analyzer (PNA) in Dr. Yoder's group. The PNA is capable for the microwave measurement from 10 MHz to 50 GHz. To test DG-HBTs, the microwave frequency was swept logarithmically between 40MHz to 20GHz for a better data resolution. The microwave power was set at -20 dBm to prevent output saturation during the measurement. The d.c bias was provided by an Agilent 4155C semiconductor parameter analyser through the bias inputs of Agilent E8364B. An Agilent VEE program was used to control the two instruments and to display the real-time measurement results. Two Cascade™ Infinity GSG probes with 150μm pitch on a Cascade™ probe station were used to probe the devices.The DG-HBTs were measured in the common-emitter coplanar waveguide (CPW) configuration. On-wafer short-open-load-through (SOLT) calibration patterns with the same dimension to the device probe pads were used to move the RF reference planes [120] to the lines indicated in Figure 24. Before each device

measurement, the on-wafer calibration was carried out using the calibration software in Agilent E8364B to prevent any possible tool variation between measurements.

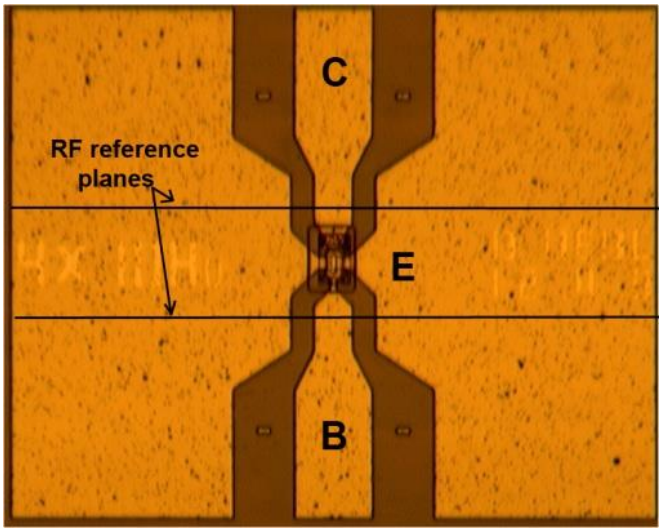

Figure 24. A microscope picture of a fabricated GaN/InGaN DG-HBT with A_E = 4 × 10 μm^2. The device is designed in G-S-G coplanar waveguide configuration for common-emitter microwave measurement.

After collecting the S-parameters at different bias conditions, the measured data was calculated in Agilent Advance Design System (ADS) software for frequency-dependent $|h_{21}|^2$, *MAG* and *U*. For the same DG-HBT (A_E = 5×20 μm^2) characterized in Figure 23, the measured frequency-dependent $|h_{21}|^2$, Mason's unilateral gain (*U)*, and *MAG* measured at V_{CE} = 13 V and J_C = 12.5 kA/cm^2 are shown in Figure 25. A 20 dB/decade line fitting is drawn on the measured $|h_{21}|^2$ curve and f_T of 8 GHz is determined. f_{max} of 1.8 GHz is determined at U = 0 dB. The stability factor (K) shows that the device is unconditionally stable for frequencies up to 20 GHz [121].

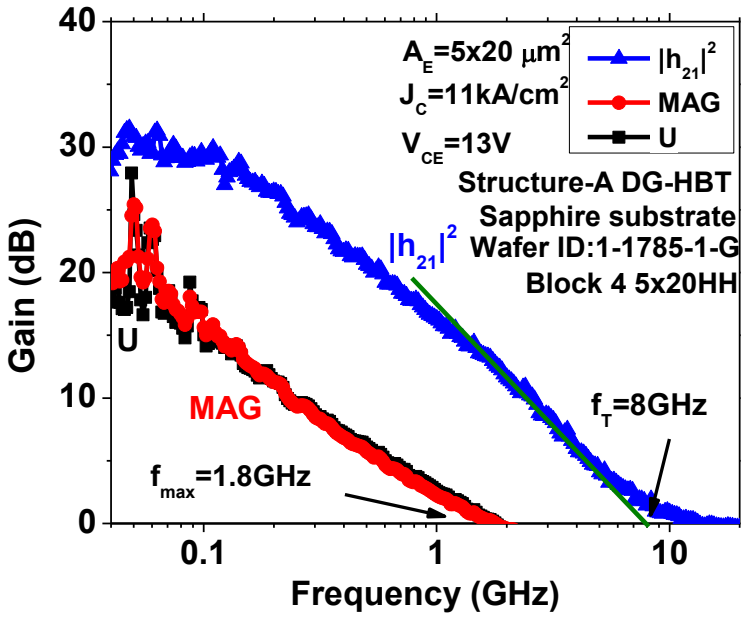

Figure 25. The measured $|h_{21}|^2$, *MAG*, and *U* of a Structure-A GaN/InGaN DG-HBT with A_E = 5×20 μm² on sapphire substrate (wafer ID: 1-1785-1-G Block4 5x20HH).

The J_C-dependent f_T and f_{max} values of the 5×20 μm² DG-HBT are plotted in Figure 26. In Figure 26 (a), f_T and f_{max} both increase with J_C and reach the maximum value of 8 GHz and 1.8 GHz respectively at $J_C > 12.5$ kA/cm². By plotting the emitter-to-collector transit time ($\tau_{ec} = 1/(2\pi f_T)$) against $1/I_C$ in Figure 26 (b), $C_{je} + C_{jc}$ = 630 fF can be extracted from the linearly-fitted slope. The base-to-collector transit time ($\tau_b + \tau_{sc} + \tau_c$) is estimated at 17 ps when one linearly extrapolates the curve to $1/I_C = 0$ as shown in Figure 26 (b). However, the devices suffer from thermal runaway and catastrophic damage at higher current stressing condition. Hence the RF characteristics were not measured for $J_C > 12.5$ kA/cm² on these DG-HBTs on sapphire substrates. Possible RF performance improvements for GaN/InGaN DG-HBTs may be achieved by further improvement in the base resistance and growing these structures on substrates with better thermal conductivity for high-current operation.

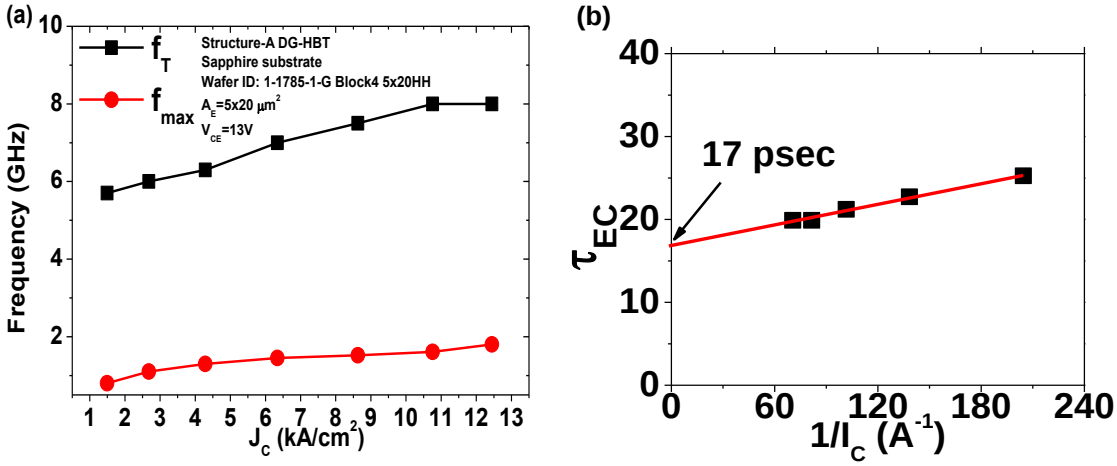

Figure 26. (a) The cut-off frequencies at different collector density (J_C) and (b) the fitted transmission time of GaN/InGaN DG-HBT with A_E = 5×20 μm^2(wafer ID: 1-1785-1-G Block4 5x20HH)

2.6.2 Small-signal model fitting and extraction

To explore the limitation of microwave performance for GaN/InGaN DG-HBTs, a hybrid-π model is developed using another Structure-A DG-HBT with f_T =5GHz, as shown in Figure 27. Using the bias condition (I_C) and current gain (β), the transconductance $g_m = qI_C/kT$ = 0.15 S and $r_\pi = \beta/g_m$ = 145 Ω can be estimated. The non-ohmic base contact is modeled by an additional R_{Bcont}. The resistance parameters such as R_{Bcont}, R_B, R_E, R_C are estimated from the TLM measurement data and the Z-parameters at low frequency. The capacitance of extrinsic BC junction and parasitic capacitance between the base and the collector contact are included in C_{BCext}. The coupling capacitance between base and emitter (C_{EBext}) is also included. C_{BE}, C_{BEext} and C_{BCext} are then estimated from the slope of τ_{ec} versus $1/I_C$. The coupling capacitance (C_{Esub}) accounts for the capacitive coupling between the emitter ground planes in the on-wafer CPW and the GaN buffer layer that is electrically connected to the sub-collector. These extracted parameters were then optimized in the Agilent Advance Design System (ADS) software and are listed in Table 8.

The plots of simulated and measured S-parameters, $|h_{21}|^2$, Mason's unilateral power gain (U) and maximum available gain (MAG) are shown in Figure 28. The simulation results (solid lines) agree well with the measured data (square data points). From the experimental data, both $|h_{21}|^2$ and U roll off at a 20 dB/decade slope. The small-signal model also indicates that the deviation of the 20 dB/decade roll-off at high frequency regime (> 2 GHz) arises from the parasitic RC network of C_{Esub}, C_{BCext}, and C_{EBext}. The parasitic components are caused by the external BC junction and the overlay of the emitter ground plane and the underlying GaN buffer layer (2500 nm thick with unintentionally doped concentration $n \sim 10^{16}$ cm^{-3}) in the common emitter coplanar waveguide test structure.

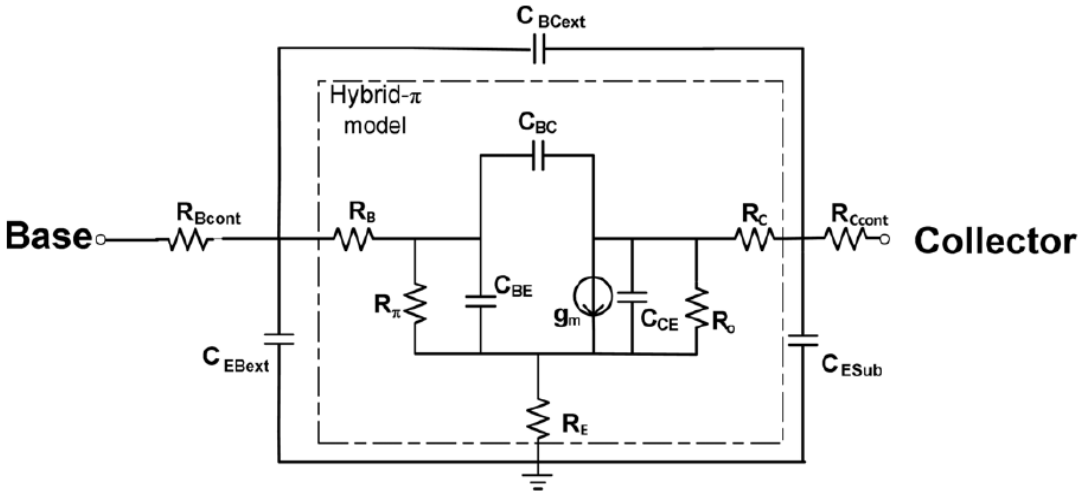

Figure 27. The schematic of small-signal circuit model of GaN/InGaN DG-HBT.

Table 8 A summary of the extracted small signal model for a GaN/InGaN DG-HBT on sapphire substrate (wafer ID: 1-1785-1-G Block4 4x20DV) at J_C = 4.7 kA cm^{-2}, V_{CE} = 7 V.

Element	Element name	Value	Element	Element name	Value
Base Schottky contact resistance	R_{Bcont}	60Ω	External BC junction capacitance	C_{BCj}	28 f F
Hybrid-π BE resistance	R_π	140 Ω	HBT transconductance	g_m	145 mS
Intrinsic BC junction capacitance	C_{BC}	55 f F	Intrinsic CE capacitance	C_{CE}	47 fF
Intrinsic BE junction capacitance	C_{BE}	640 f F	HBT Output resistance	R_o	1.2kΩ
Base resistance	R_B	2.5 k Ω	Emitter resistance	R_E	110Ω
Collector resistance	R_C	175Ω	Collector contact resistance	R_{Ccont}	20Ω
Coupling capacitor between emitter to sub-collector	C_{ESub}	65 f F	Coupling capacitor between emitter to external base	C_{EBext}	1 f F

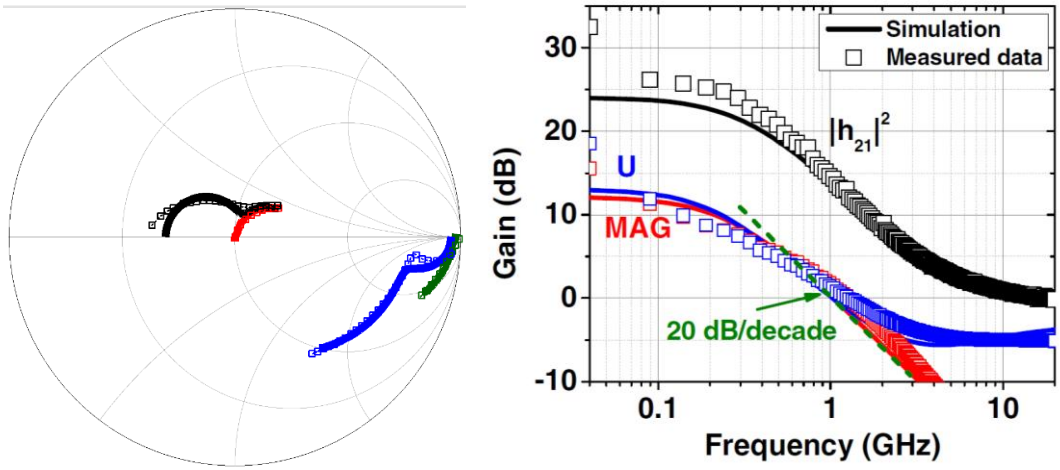

Figure 28. (a) The measured (lines with squares) and simulated (solid lines) of the S-parameter fitting and (b) the measured versus simulated $|h_{21}|^2$, *MAG* and *U* for a 4 × 20 μm^2 GaN/InGaN DG-HBT (wafer ID: 1-1785-1-G Block 4 4x20DV) at V_{CE} = 7 V and J_C = 4.7 kA cm^{-2}.

Other than the parasitic components, the fabricated DG-HBTs also suffer from high collector and emitter resistance, which may come from the degradation of the metal stacks after repeated current stressing. The base resistance is also unusually high due to the non-ohmic base contact. If these high resistance components are replaced with typical

resistance values (2 Ω for R_C and R_E, and 300 Ω for R_B), the simulated f_T and f_{max} would have been 31 GHz and 90 GHz, respectively, as shown in Figure 29. Given the current device layout, to achieve R_B < 300 Ω, the specific base contact resistance and base sheet resistance (R_{sheet}) needs to be lower than 4E-4 Ω-cm^2 and 18 kΩ/□, respectively. Similarly, to achieve R_E and R_C < 2 Ω, the specific emitter and collector contact resistance has to be smaller than 1.2E-6 Ω-cm^2 and 9E-6 Ω-cm^2, respectively. Therefore, further improvement in ohmic contact resistance and aggressive device down scaling would be necessary to improve the RF performance of GaN/InGaN DG-HBTs.

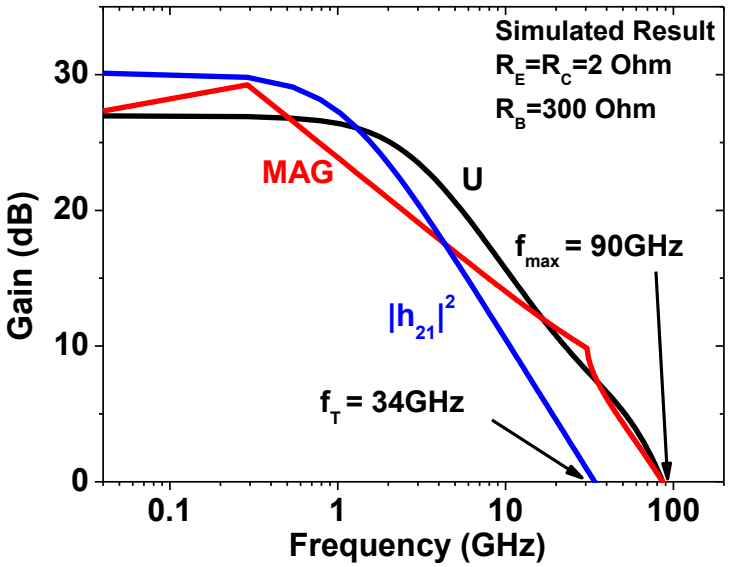

Figure 29. The simulated $|h_{21}|^2$, *MAG* and *U* for a GaN/InGaN DG-HBT with R_C = R_E = 2Ω and R_B =300Ω.

Based on the small-signal model and the measured breakdown voltage, the Johnson's figure of merit (JFOM) for GaN/InGaN DG-HBT could be estimated as high as 5 THz-V ($f_T \cdot BV_{CEO}$ > 34 GHz × 155 V). This JFOM validates the prediction that III-N HBTs could be a promising transistor platform for future THz technologies [122]. As shown in Figure 30, the JFOM of the microwave GaN/InGaN DG-HBTs developed at Georgia Tech, however, is still about an order of magnitude lower than the expected

performance. The result suggests that further improvement in contact resistance and device scaling are required to achieve better microwave performance on *npn* GaN/InGaN DG-HBTs.

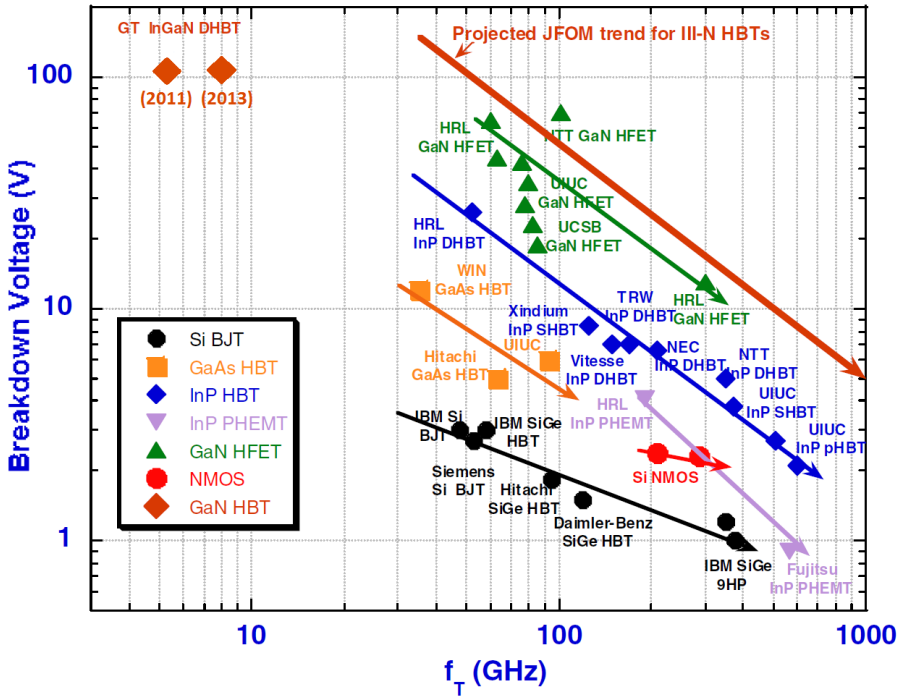

Figure 30. The summarized f_T-BV trend (JFOM) for each semiconductor technology [95].

2.7 Summary

In summary, high-performance *npn* GaN/InGaN DG-HBTs were developed and studied at Georgia Tech. Nitrogen-incorporated dry etching processes and Pd-based *p*-type base contacts were developed to improve device performance and device stability. The impact of indium content in base layer, substrate materials, and a constant-current stress were studied to improve the performance of GaN/InGaN DG-HBTs. With those studies and process optimization, high current gain (h_{fe}>110), high current density (J_C > 141 kA/cm^2), and high power density (P_{dc} > 3MW/cm^2) were achieved on the GaN/InGaN DG-HBTs grown on a FS-GaN substrate. The GaN/InGaN DG-HBTs grown

on a sapphire substrate also achieved J_C > 95 kA/cm^2 and P_{dc} > 1.3MW/cm^2. To our best knowledge, the results are state-of-the-art current gain, current density, power density than other III-N HBTs to date. High-temperature operation capability up to 250C was also demonstrated by DG-HBTs on FS-GaN substrates. High cut-off frequencies f_T > 8GHz and f_{max} > 1.8GHz were measured for DG-HBTs grown on sapphire substrates. With the measured S-parameters, the first small-signal model for III-N DG-HBTs was developed. These results clearly indicate the capability and feasibility of III-N DG-HBTs for future high-power and high-frequency applications.

Based on the results in this study, eleven journal papers [95, 106, 113, 119, 121, 123, 124, 125, 126, 127] [128] and eight conference papers [129, 130, 131, 132, 133, 134, 135, 136] were published.

CHAPTER 3

DEVELOPMENT OF III-N HETEROJUNCTION FIELD-EFFECT TRANSISTOR

3.1 Introduction

III-N heterojunction field-effect transistors (HFETs) have also been intensively studied in recent years for high-power and microwave applications. The strong polarization and wide bandgap enable III-N HFETs to achieve high current drive, high cut-off frequency and high breakdown voltage. However, high contact resistance is still a major issue for III-N HFETs for achieving better current drive and cut-off frequency. Normally-on characteristics also prevent the application to the existing power systems due to safety concerns. Current-collapse caused by carrier trapping degrades the switching performance of III-N HFETs. In this chapter, the objective is to present the simulation results, process improvement and the device characterization for III-N HFETs developed at Georgia Tech to achieve lower contact resistance, uniform V_{th} control and effective surface passivation.

Before actual fabrication processes, a semiconductor device simulator (Synopsys Sentaurus Device) is used to study different AlGaN layer thickness and recessed-gate structure for d.c and microwave performance to explore a better design for III-N HFETs. The simulated results suggest that a thinner AlGaN layer leads to a more positive threshold voltage (V_{th}) but causes degradation of cut-off frequency f_T. To achieve a higher f_T with a more positive V_{th}, a recessed-gate structure is simulated and proven to be more preferred than a thin AlGaN layer structure. Therefore, recessed-gate structure is chosen

to control the V_{th} of III-N HFETs in this study. The impact of source-field plate (SFP) is also simulated to explore possible improvement in breakdown voltage of III-N HFETs. The results show that an additional SFP helps reduce the peak electric field in HFETs. However, a high electric field is observed at SFP edge at drain side. Therefore, an optimal SFP length of 0.75 to 1.5 μm is desired to reduce the peak electric field for higher breakdown voltage of III-N HFETs. The simulated results still provides a possible approach to improve the breakdown voltage of III-N HFETs in the future.

For the process development, an in-situ doped metal contact scheme was developed to achieve 50% lower contact resistance than typical Ti/Al-based metal contacts. A unique photo-enhanced electrode-less wet etching technique was developed to prevent possible plasma etching damage for recessed-gate III-N HFETs. An AlN layer in the epitaxial structure serves as an etch-stop layer to achieve a uniform recess depth across the sample. With the electrode-less wet etching, V_{th} = 0.06 V with standard deviation < 0.17 V was measured out of 60 fabricated recessed-gate AlGaN/AlN/GaN HFETs with gate width (W_G) = 3 mm to 10 mm. The quasi-static family curves shows a maximum current drive > 4 A at V_{GS} = 4 V. The minimal specific on-resistance $R_{on}{\cdot}A$ is < 6 mΩ-cm^2 with the breakdown voltage of recessed-gate > 1200 V measured on a HFET with L_{GD} = 13 μm. It corresponds to a figure of merit (BV^2/R_{on}) of 240 MW/cm^2 which is among the best reported normally-off III-N HFETs.

A remote-oxygen-plasma treatment in a plasma-enhanced atomic-layer deposition (PE-ALD) system was proposed and demonstrated beneficial to improve current-collapse and high dynamic on-resistance for III-N HFETs. With the remote-oxygen-plasma treatment, a 0.25 V threshold voltage shift is measured without any carrier density

degradation in the 2DEG channel of recessed-gate AlGaN/AlN/GaN HFETs. Current-collapse in the gate-pulsed family curves is eliminated by the remote-oxygen-plasma treatment. The dynamic on-resistance of recessed-gate HFETs is reduced by 67 % after the oxygen plasma treatment.

To explore better d.c and microwave performance, InAlN/AlN/GaN HFETs with sub-micron T-gate length (L_G = 150 nm) without recess etching were also fabricated and characterized at Georgia Tech. The maximum current drive $I_{D,max}$ = 1.4 A/mm and a maximum transconductance ($g_{m,max}$) of 250 mS/mm are achieved. The maximum cut-off frequency f_T of 80 GHz and f_{max} of 106 GHz are measured on a 2×50-μm-wide device. The product of cut-off frequency and gate length ($f_T \times L_G$) is 12 GHz-μm. These results not only indicate performance improvement by using InAlN/AlN/GaN hetero-structures but also validate the developed fabrication processes on different III-N HFETs.

3.2 Device fundamentals

III-V HFETs, such as GaAs-based HFETs [137] and InP-based HFETs [138], have been widely used for microwave applications today. For III-V HFETs, the 2DEG channel is achieved by a modulation-doped or delta-doped epitaxy layer grown by MBE or MOCVD systems. However, for III-N HFETs, the 2DEG channel can be achieved by the spontaneous polarization (P^{SP}) and piezoelectric polarization (P^{PE}) in III-N materials without any intentional doping. The P^{SP} of III-N materials is caused by the intrinsic asymmetry of the bonding in wurtzite crystal structure of III-N materials. The measured values of spontaneous polarization of III-N materials are summarized in Table 9.

Table 9 The summary of measured spontaneous polarization of III-N materials

Spontaneous polarization P^{SP}(C/m^2)			
GaN	AlN	InN	Ref.
-0.029	-0.081	-0.032	[139]
-0.034	-0.090	-0.042	[140]

Because III-N materials have larger piezoelectric constants than III-V and II-VI semiconductors [141], the piezoelectric polarization of a strained III-N layer has to be taken into consideration for III-N heterojunctions. Assuming a III-N material layer is linear elastic, the relation of piezoelectric polarization tensor [P^{PE}] and strain tensor [ε] can be described as:

$$[P^{PE}] = [e][\varepsilon] \tag{26}$$

,where [P^{PE}] is the 3 × 1 matrix for piezoelectric polarization in x,y and z direction. [e] is the piezoelectric coefficients which is a 3 × 6 matrix for III-N materials. [ε] is the 6 × 1 matrix for the strain of the elastic material. Because of the wurtzite lattice symmetry of III-N materials, the [e] tensor can be reduced to only 3 independent piezoelectric coefficients and the piezoelectric polarization [P^{PE}] can be expressed as [142]:

$$\begin{pmatrix} P_x^{PE} \\ P_y^{PE} \\ P_z^{PE} \end{pmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{bmatrix} \begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{yz} \\ \varepsilon_{xz} \\ \varepsilon_{xy} \end{pmatrix} = \begin{pmatrix} e_{15}\varepsilon_{xz} \\ e_{15}\varepsilon_{yz} \\ e_{31}(\varepsilon_{xx} + \varepsilon_{yy}) + e_{33}\varepsilon_{zz} \end{pmatrix} \tag{27}$$

The piezoelectric coefficient e_{15} is related to the polarization induced by a shear strain which is not applicable to the typical epitaxial growth scheme along the *c*-axis for typical Ga-polar AlGaN/GaN and InAlN/GaN hetero-structures [143]. As a result, only the piezoelectric polarization along the *c*-axis (P_z^{PE}) of the wurtzite crystal is considered.

The strain in the *x* and *y* directions can also be assumed the same (ε_{xx}=ε_{yy}) because of the symmetry of the hexagonal lattice structure. Therefore, the total piezoelectric polarization (P^{PE}) in a strained III-N layer can be expressed as:

$$P^{PE} = P_z^{PE} = 2e_{31}\varepsilon_{xx} + e_{33}\varepsilon_{zz} \tag{28}$$

,where $\varepsilon_{xx} = (a - a_0)/a_0$ and $\varepsilon_{zz} = (c - c_0)/c_0$. The a and c are the strained lattice constants of wurtzite lattice structure while a_0 and c_0 are the unstrained values. For a thin epitaxial III-N film grown on a thick substrate, the lattice constant a of the epitaxial layer is strained to match the value in the substrate. Therefore, the lattice constant c is then determined by the minimal energy with respect to the perpendicular strain. Therefore, the change of lattice constants can be determined by the stiffness constants as:

$$\varepsilon_{zz} = -2\frac{C_{13}}{C_{33}}\varepsilon_{xx} \tag{29}$$

Therefore, the total piezoelectric polarization in Equation (28) can be revised to [144]:

$$P^{PE} = 2\varepsilon_{xx}\left(e_{31} - 2e_{33}\frac{C_{13}}{C_{33}}\right) = 2\frac{a - a_0}{a_0}\left(e_{31} - 2e_{33}\frac{C_{13}}{C_{33}}\right) \tag{30}$$

For III-N materials, the unstrained lattice constants (a_0), polarization coefficients (e) and stiffness constants (C) have been calculated theoretically or measured experimentally as summarized in Table 10. For ternary III-N semiconductors, such as AlGaN and InAlN, the unstrained lattice constants (a_0), polarization coefficients (e) and stiffness constants (C) and spontaneous polarization (P^{SP}) can be approximated by Vegard's law [3].

Table 10 The summary of lattice constants, piezoelectric polarization coefficients and stiffness constants for III-N materials

	GaN	AlN	InN	Ref.
a_0 (Å)	3.189	3.112	3.54	[145]
e_{31} (C/m^2)	-0.49	-0.6	-0.57	[140]
	−0.34	−0.53	−0.41	[146]
e_{33} (C/m^2)	0.73	1.46	0.97	[140]
	0.67	1.50	0.81	[146]
		1.55		[147]
C_{13} (GPa)	103	108	92	[148]
	110	100		[149]
	120	70	121	[52]
C_{33} (GPa)	405	373	224	[148]
	390	390		[149]

For an actual III-N heterojunction, the strained III-N layer may be partially relaxed. Therefore, a relaxation factor (*relax*) has to be taken into consideration and the Equation (30) is modified as:

$$P^{PE} = 2\frac{a - a_0}{a_0} \times relax \times \left(e_{31} - 2e_{33}\frac{C_{13}}{C_{33}}\right) \tag{31}$$

,where *relax* = 1 for a fully strained layer and = 0 for a fully relaxed layer. The total polarization (*P*) in a III-N layer is the sum of the spontaneous polarization and the piezoelectric polarization:

$$P = P^{SP} + P^{PE} \tag{32}$$

Depending on the stress of III-N material, P^{PE} may be parallel or antiparallel to the P^{SP}. For example, For a Ga-polar AlGaN layer grown on a GaN substrate, a tensile strain applied on the AlGaN layer produces the P^{PE} in parallel to the P^{SP} pointing toward to the substrate as shown in Figure 31.

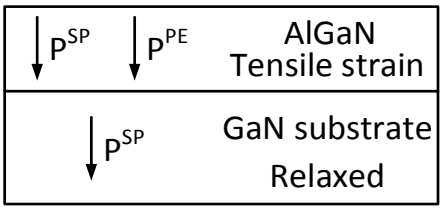

Figure 31. The directions of the spontaneous and piezoelectric polarization in Ga-polar tensile-strained AlGaN/GaN heterostructure.

The polarization-induced charge density (σ_P) can then be calculated from the gradient of total polarization P by:

$$\sigma_P = -\nabla P \tag{33}$$

At an abrupt interface of III-N heterostructure, P can decrease or increase within a bilayer, causing a high density of polarization-induced charge at the hetero-interface [144]:

$$\begin{aligned} \sigma_P &= P(top) - P(bottom) \\ &= \{P^{SP}(top) - P^{SP}(bottom)\} + \{P^{PE}(top) - P^{PE}(bottom)\} \end{aligned} \tag{34}$$

If the polarization-induced charge density (σ_P) is positive, electron accumulate and form a 2-dimensional electron gas (2DEG) at the hetero-interface. Therefore, a highly strained AlGaN/GaN or AlN/GaN heterojunction is preferred for achieving a higher 2DEG carrier density for III-N HFETs.

In addition to the polarization-induced electron, the sheet electron density (n_s) at 2DEG is also affected by the band diagram of the III-N heterojunction. For a band diagram of an AlGaN/GaN heterojunction with a Schottky gate contact at 0V as shown in Figure 32, the n_s can be expressed as:

$$n_s = \frac{\sigma_P}{q} - \frac{\varepsilon_{AlGaN}}{q d_{AlGaN}} \left(\phi_B - \Delta E_C + E_{f0} \right) \tag{35}$$

,where σ_P is the polarization-induced electron density. ε_{AlGaN} is the permittivity of AlGaN layer. d_{AlGaN} is the AlGaN thickness. ϕ_B is the Schottky barrier height of the Schottky gate.

ΔE_C is the conduction band offset at the AlGaN/GaN interface. E_{f0} is the Fermi level with respect to the GaN conduction band.

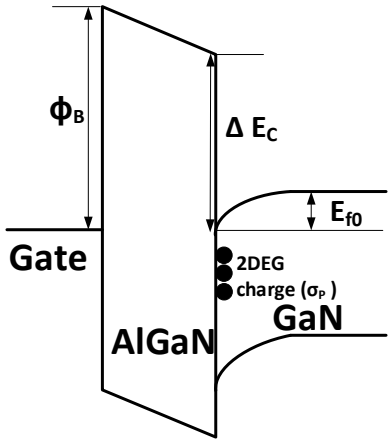

Figure 32. The band diagram of AlGaN/GaN heterojunction at 0V.

Therefore, the threshold voltage (V_{th}) of AlGaN/GaN HFETs can be expressed as:

$$V_{th,Schottky} = -\frac{d_{AlGaN}}{\varepsilon_{AlGaN}} n_s = \frac{\phi_B}{q} - \frac{\Delta E_C}{q} + \frac{E_{f0}}{q} - \frac{d_{AlGaN}}{\varepsilon_{AlGaN}} \sigma_P \quad (36)$$

For III-N HFETs, σ_P can be higher than 1E13 cm^{-2} due to the strong polarization of III-N materials [52]. A thicker AlGaN barrier (d_{AlGaN} > 20nm) is also preferred for lower gate leakage current. Therefore, the negative term of σ_P usually dominates and results in a negative V_{th} value for normally-on (Depletion-mode) III-N HFETs. However, in the perspective of circuit design, normally-off characteristics (Enhancement-mode) III-N HFETs are still preferred.

In the past few years, several approaches have been successfully demonstrated to adjust V_{th} of III-N HFETs. *P*-type III-N gate electrode has been proposed to adjust ϕ_B for different V_{th} [71]. By adding a gate metal with high work function on *p*-type III-N gate, normally off characteristics with different V_{th} can be achieved [150]. However, a complex selective regrowth process or an etching process have to be used to pattern the *p*-type III-

N gate. Non-uniform regrowth or etching damage may be very challenging for wafer level processing. Fluorine-implantation under gate electrode has also been demonstrate to adjust V_{th} of III-N HFETs [70, 151]. Fluorine implants in AlGaN layer serve as modulation doping in barrier layer to adjust to achieve the desired V_{th}. Fluorine implantation process, however, causes implantation damage to III-N barrier layer, resulting in increased gate leakage current and shorter device lifetime. The vacancies induced by ion implantation also degrades the stability of fluorine dopant in III-N materials [152]. Another approach using a tunnel junction structure with a Schottky barrier at source contact was also proposed [73]. However, the achievable V_{th} is limited by the Schottky barrier height at the source contacts.

In addition to those approaches, recessed-gate structure is also considered as an effective approach to control V_{th} by recessing the AlGaN layer (d_{AlGaN}) under the gate electrode. Different V_{th} can be achieved on the same sample by controlling recess depth in different devices. This gives a great flexibility for E/D-mode III-N MMIC design and integration. In addition, at $V_{DS} > V_{GS}-V_{th}$, the transconductance (g_m) of HFETs can be expressed as: [93]

$$g_m = \frac{W_G C_{gg} \mu}{L_G}(V_{GS} - V_{th}) \tag{37}$$

,where W_G is the gate width. L_G is the gate length. μ is the carrier mobility. C_{gg} is the normalized intrinsic gate capacitance. V_{GS} is the gate-to-source voltage and V_{th} is the threshold voltage. By reducing d_{AlGaN} in recessed-gate structure, a higher g_m can be achieved than other V_{th}-control approaches.

For high-power switching applications, lower on-resistance (R_{on}) is desired to reduce switching loss and power dissipation at the on-state. The on-resistance (R_{on}) of HFETs at linear region can be separated into four terms [153] :

$$R_{on} = R_S + R_{ch} + R_D + 2R_{cont} = \frac{L_{GS}}{q\mu n_s} + \frac{L_G d_{AlGaN}}{\mu\varepsilon_{AlGaN}(V_{GS} - V_{th})} + \frac{L_{GS}}{q\mu n_s} + 2\frac{\rho_{cont}}{L_{cont}} \quad (38)$$

,where R_S and R_D are the gate-to-source and gate-to-drain access resistance, respectively, which are determined by the gate-to-source distance (L_{GS}), gate-to-drain distance (L_{GD}), carrier mobility (μ) and 2DEG carrier density (n_s). R_{ch} is the intrinsic channel resistance under gate electrode, which depends gate length (L_G), gate capacitance (C_{gg} = $d_{AlGaN}/\varepsilon_{AlGaN}$), gate voltage ($V_{GS}$) and threshold voltage (V_{th}). R_{cont} is the contact resistance of drain and source contacts which can be calculated by the specific contact resistance (ρ_C) and transfer length (L_{cont}).

According to Equation (38), smaller device dimensions ($L_{GD,}$ L_{GS} and L_G) are preferred for lower R_{on}. However, the breakdown voltage (*BV*) is usually proportional to L_{GD}. A small L_G would also results in high drain leakage caused by short-channel effect [154] . As a result, a design trade-off exists between R_{on} and *BV*. For recessed-gate III-N HFETs, only R_{ch} is altered by different recess depth while the polarization-induced 2DEG channel enables high n_s and μ to reduce R_{GS} and $R_{GD.}$ The wide bandgap of III-N materials also provide higher *BV* than III-V HFETs and silicon MOSFETs. Therefore, in this study, we focused on the development of recessed-gate III-N HFETs for high-voltage and high-power switching applications.

Nevertheless, recess etching damage and recess uniformity are the major issues for recessed-gate structure. A low-damage uniform etching process is required to achieve

uniform recess depth without etching damage for the recessed-gate HFETs. At Georgia Tech, a unique electrode-less wet etching is developed for recessed-gate etching to eliminate the etching damage. AlN layer serves as the etching-stop layer to achieve uniform recessed depth across the sample. The detailed results will be discussed in the following sections.

In addition to high-power performance, the polarization-induced 2DEG channel also enhances carrier saturation velocity (v_{sat}) for III-N HFETs. Therefore, a higher Johnson's figure-of-merit (JFoM) is expected for III-N HFETs than other microwave FETs. When considering all the parasitics, the unity current gain frequency f_T for HFETs can be expressed as [93]:

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{\left[1+\left(1+g_m\left(R_S+R_D\right)\right)\frac{C_{gd}}{C_{gs}}\right]^2-\left[\left(1+g_m R_S\right)\frac{C_{gd}}{C_{gs}}\right]^2}} \tag{39}$$

,where g_m is the transconductance. C_{gd} and C_{gs} are the gate-to-drain and gate-to-source capacitance, respectively, which are proportional to gate length (L_G). R_S and R_D are the source and drain resistance. The terms of R_C and R_D suggest that smaller L_{GD} and L_{GS} are preferred to improve f_T. Lower contact resistance is also required. The C_{gg} related to the gate length (L_G) suggests that L_G needs to be small. In addition, as shown in Equation (37,) g_m is also reversely proportional to L_G. As a result, f_T is proportional to $1/L_G^2$ and a sub-micron gate electrode is desired to achieve higher f_T for HFETs. For microwave FETs, the $f_T \times L_G$ product is typically used to evaluate the microwave performance.

When considering the parasitics, the maximum oscillation frequency f_{max} of HFETs can be expressed as [93]:

$$f_{\max} = \frac{f_T}{2\sqrt{2\pi f_T R_G C_{gd} + g_{ds}(R_G + R_S)}} \quad (40)$$

,where R_G is the gate resistance. g_{ds} is the drain conductance (= $dI_D/dV_{DS.}$) The equation of f_{max} suggests that a wider gate electrode is preferred for lower gate resistance (R_G) and higher f_{max}. Therefore, different shapes of gate electrode, such as T-shaped or Γ-shaped gate, are proposed for smaller gate capacitance and lower R_G to achieve high f_T and f_{max} simultaneously.

In addition to device design, g_m, C_{gs} and C_{gd} are also affected by layer structure of HFETs. To take the influence of different layer structure into consideration, Synopsys Sentaurus Device simulator is used to simulate d.c transfer curves and microwave characteristics of HFETs with different AlGaN thickness and recessed-gate structure. To further enhance the *BV* of HFETs, gate-field plate (GFP) and source-field plate (SFP) structure have been successfully demonstrated on various devices [155, 156]. However, GFP potentially degrades microwave and switching performance due to larger gate capacitance. On the other hand, SFP is considered more flexible for device design to enhance *BV*. Nevertheless, exploring an optimal SFP dimension by actual device fabrication with different SFP designs is time-consuming and not cost-effective. Therefore, the influence of different SFP dimensions to the electric distribution of HFETs is also simulated in Synopsys Sentaurus Device simulator to obtain the optimal SFP design. The detailed simulation results will be discussed in the following section.

Compared to AlGaN/GaN HFETs, InAlN/GaN HFETs provide higher current drive, higher g_m and lower access resistance due to the higher spontaneous polarization of InAlN layer. Lattice-matched InAlN layer is also achievable on GaN substrate to

eliminate lattice-mismatch-induced defects. At Georgia Tech, we collaborate with AMDG group led by Prof. Dupuis to develop microwave InAlN/AlN/GaN HFETs. Although our studies reveal the unintentional incorporation (auto-doping) of Ga during InAlN growth [157, 158], which degrades device performance, the fabricated InAlN/AlN/GaN HFETs are still demonstrated with 1.4 A/mm current drive and f_T > 80GHz. The detailed measurement results will be included in the following sections.

3.3 III-N HFET simulation

Before actual device fabrication, Synopsys Sentaurus Device simulator was used to study different AlGaN thickness, recessed-gate structure and source-field plate designs for III-N HFETs. The device simulation helps study more process variation for optimizing device designs and provides more insight to the electric properties of III-N HFETs before actual device fabrication.

3.3.1 Relaxation factor calibration

To simulate III-N HFETs, the parameters listed in Table 9 and Table 10 are included in the piezoelectric polarization model in Sentaurus simulator to calculate the polarization-induced 2DEG in III-N HFETs. The Poisson and carrier continuous equations are also included in the simulation. However, for actual AlGaN/AlN/GaN HFETs, AlGaN barrier layer may be partially relaxed. To extract the relaxation factor for a more accurate simulation, *C-V* and *I-V* simulations were carried out on an AlGaN/AlN/GaN structure and compared to the experimental data from the AlGaN/AlN/GaN wafer (wafer ID: GA0633-35). The simulated AlGaN/AlN/GaN structure consists of 25nm $Al_{0.2}Ga_{0.8}N$ barrier layer, a 1nm AlN layer and a 3μm GaN

buffer layer, which is the same to GA0633-35 wafer. The simulated HFETs has L_{GD} = 8.5 μm, L_G = 3 μm and L_{GS} = 2 μm. 5.3eV work-function is assign to the gate electrode to simulate the nickel gate. 10 Ω contact resistance are also used in the simulation.

In Figure 33 (a), the simulated *C*-*V* curves with 20%-relaxed AlGaN layer (*relax* = 0.2) show a good agreement in threshold voltage (V_{th} = -2.5 V) and gate capacitance to the experimental data. In the I_D-V_{GS} transfer curves in Figure 33 (b), consistent V_{th} and sub-threshold slope (*S*) are observed. The higher on-state current in the simulated I_D-V_{GS} transfer curves is attributed to the lower contact resistance assigned in the simulation. Because the Schottky gate leakage current is not included in the simulation, the simulated off-state leakage current is lower than the experimental results. Nevertheless, the results suggest that the simulated layer structure with 20 % relaxation is close to the actual AlGaN/AlN/GaN heterostructure.

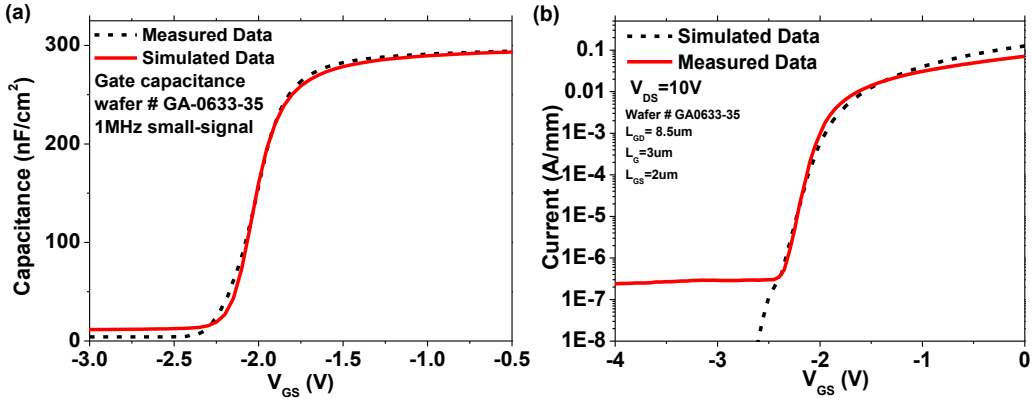

Figure 33. The simulated and measured (a) *C*-*V* and (b) I_D-V_{GS} results of the AlGaN/AlN/GaN HFETs.

3.3.2 Study of AlGaN barrier thickness

In Equation (37), a thinner AlGaN layer results in higher gate capacitance (C_{gg}) and increased intrinsic transconductance (g_m). Higher g_m is preferable to achieve higher f_T

while larger C_{gs} and C_{gd} degrades f_T based on Equation (39). Thus a software simulation is required to take all the effects into consideration for extrinsic g_m and f_T. In this study, AlGaN/AlN/GaN HFETs with three different AlGaN thickness (d_{AlGaN} = 25nm, 15nm and 10nm) were simulated for I_D-V_{GS} transfer curves and the extrinsic g_m curves as shown in Figure 34. The simulated HFETs has L_{GD} = 4 μm, L_G = 0.5 μm and L_{GS} = 2 μm. The simulated I_D-V_{GS} transfer curves show that the V_{th} shifts toward positive from -2.3 V to -0.4 V when AlGaN thickness is reduced. However, the simulated peak extrinsic g_m only slightly increases from 186 mS/mm to 191 mS/mm. When AlGaN thickness is further reduced to 10nm, the peak g_m value drops to 181mS/mm. The results are attributed to the increased drain and source access resistance when AlGaN layer thickness is reduced. Therefore, the simulated peak f_T is reduced from 22 GHz to 18 GHz at V_{DS} = 10V when AlGaN layer thickness is reduced from 25 nm to 10nm as shown in Figure 35.

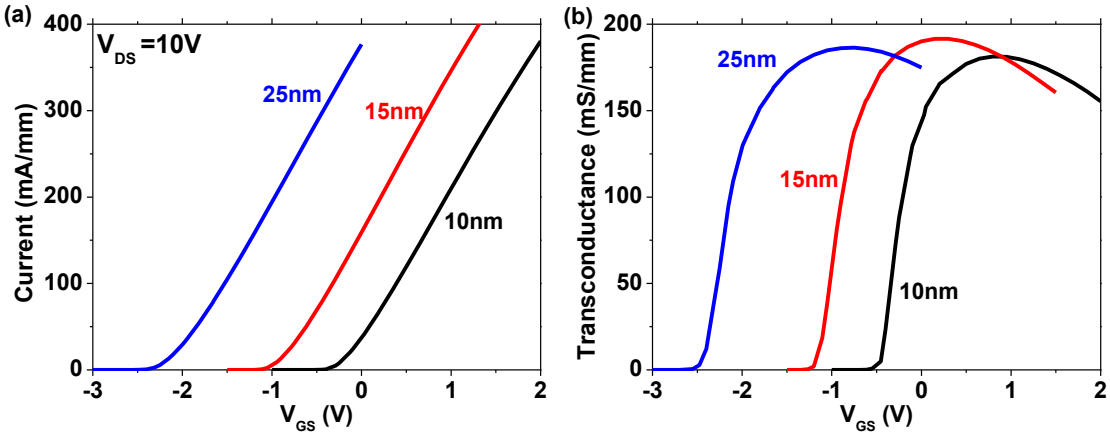

Figure 34. The simulated (a) I_D-V_{GS} transfer curves and (b) transconductance (g_m) of AlGaN/AlN/GaN HFETs with different AlGaN thickness at V_{DS} = 10V

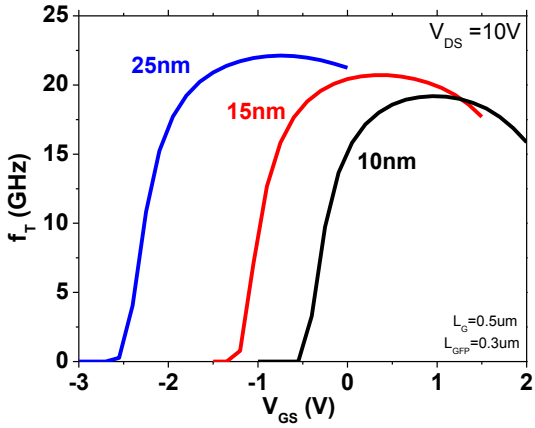

Figure 35. The simulated f_T of AlGaN/AlN/GaN HFETs with different AlGaN thickness at V_{DS} = 10V

3.3.3 Study of recessed-gate structure

In the previous simulation results, a thinner AlGaN layer leads to a more positive V_{th} but a reduced f_T. To achieve a more positive V_{th} without f_T degradation, a recess-gate structure could be a better solution. An AlGaN/AlN/GaN HFET with 15 nm recess under the gate region are simulated and compared to the results without recess. The simulated HFETs has L_{GD} = 4 μm, L_G = 0.5 μm and L_{GS} = 2 μm. In Figure 36, the simulated I_D-V_{GS} transfer curves of the recessed-gate AlGaN/AlN/GaN HFET shows a more positive V_{th} of -0.7 V than -2.3 V on the as-grown AlGaN/AlN/GaN HFET. The peak extrinsic g_m is also increased from 180mS/mm on the as-grown HFET to 248 mS/mm on the recessed-gate HFET. The results indicate that recessed-gate structure helps achieve a more positive V_{th} with a higher g_m.

Although the peak g_m is increased by the recessed-gate structure, the recessed-gate structure also results in higher gate capacitance (C_{gs} and C_{gd}). As a result, similar peak f_T values (22 GHz) are observed on the recessed-gate and as-grown HFETs as shown in Figure 37. Although f_T is not improved on the recessed-gate HFETs, the results

suggest that a recessed-gate structure is preferable than using a thin AlGaN layer to achieve a more positive V_{th} for III-N HFETs.

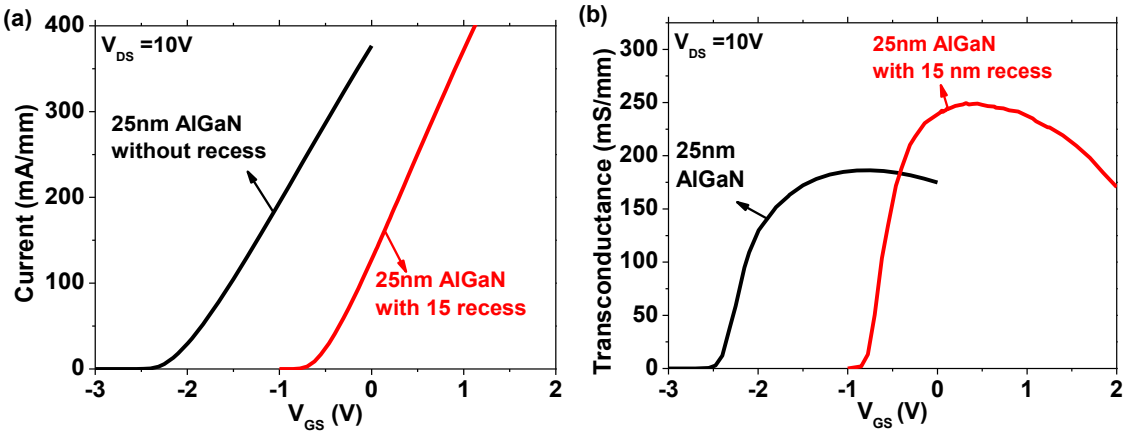

Figure 36. The simulated (a) I_D-V_{GS} transfer curves and (b) g_m of AlGaN/GaN HFETs with and without recess.

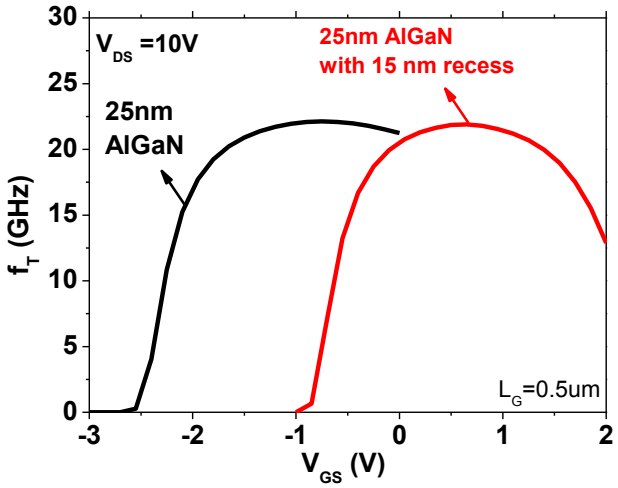

Figure 37. The simulated f_T of AlGaN/AlN/GaN HFETs with and without recess.

In summary, the simulation results clearly indicate that the recessed-gate structure is more preferable to achieve a more positive V_{th} with a better extrinsic g_m. Thus in this study, we focused on the development of recessed-gate III-N HFETs for normally-off operation. The experimental results will be discussed in the following sections.

3.3.4 Study of source-field plate

In addition to microwave performance, a high breakdown voltage (*BV*) is required for III-N HFETs. To enhance BV, source-field plate (SFP) is considered advantageous the gate-field plate (GFP) in terms of design flexibility. However, the influence and the optimal design of SFP are difficult to obtain by actual device fabrication. Therefore, in this study, the electric field of AlGaN/AlN/GaN HFETs with different SFP length from 0.5μm to 3μm were simulated and compared to the HFETs without SFP. The schematics of III-N HFETs with and without SFP are shown in Figure 38. The simulated HFETs have L_{GD} = 7.5 μm, L_G = 2 μm and L_{GS} = 1.5 μm. The gate top is 3μm-long. The SFP length (SFP_D) varies from 0.25 to 3 μm in this simulation. 250 nm-thick SiN layer with a dielectric constant (ε_{SiN}) of 6.5 is used as the insulator for SFP.

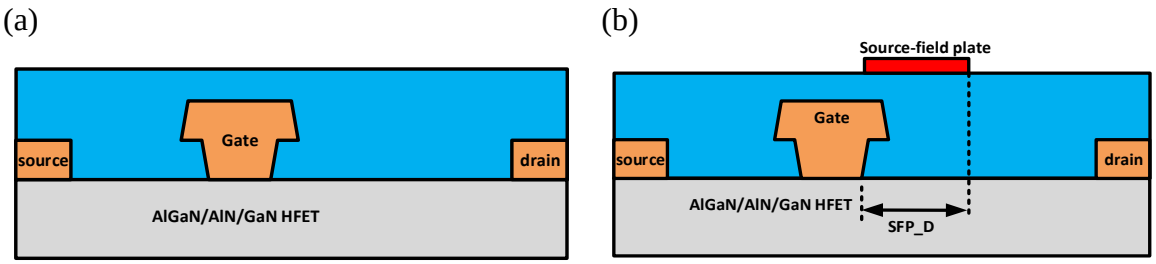

Figure 38. The schematic of AlGaN/AlN/GaN HFET (a) without SFP (b) with SFP

At V_{GS} = -5V and V_{DS} = 500V, the simulated electric field distribution along the AlGaN surface and 2DEG channel of HFETs with different SFP dimension are shown in Figure 39. It can be seen that the electric field near gate edge is reduced when a longer SFP is used. However, another high field region is observed at the edge of SFP. The electric field at SFP edge increases and exceeds that at gate edge when SFP is longer than 0.5 μm. Therefore, the result indicates that a long SFP is not preferred. The optimal

length of SFP is around 0.5 ~ 1 μm to achieve low electric field at the gate and SFP edges simultaneously. The simulation results provide a viable approach to improve the breakdown voltage of III-N HFETs. Further study on SFP structures are required for III-N HFETs in the future.

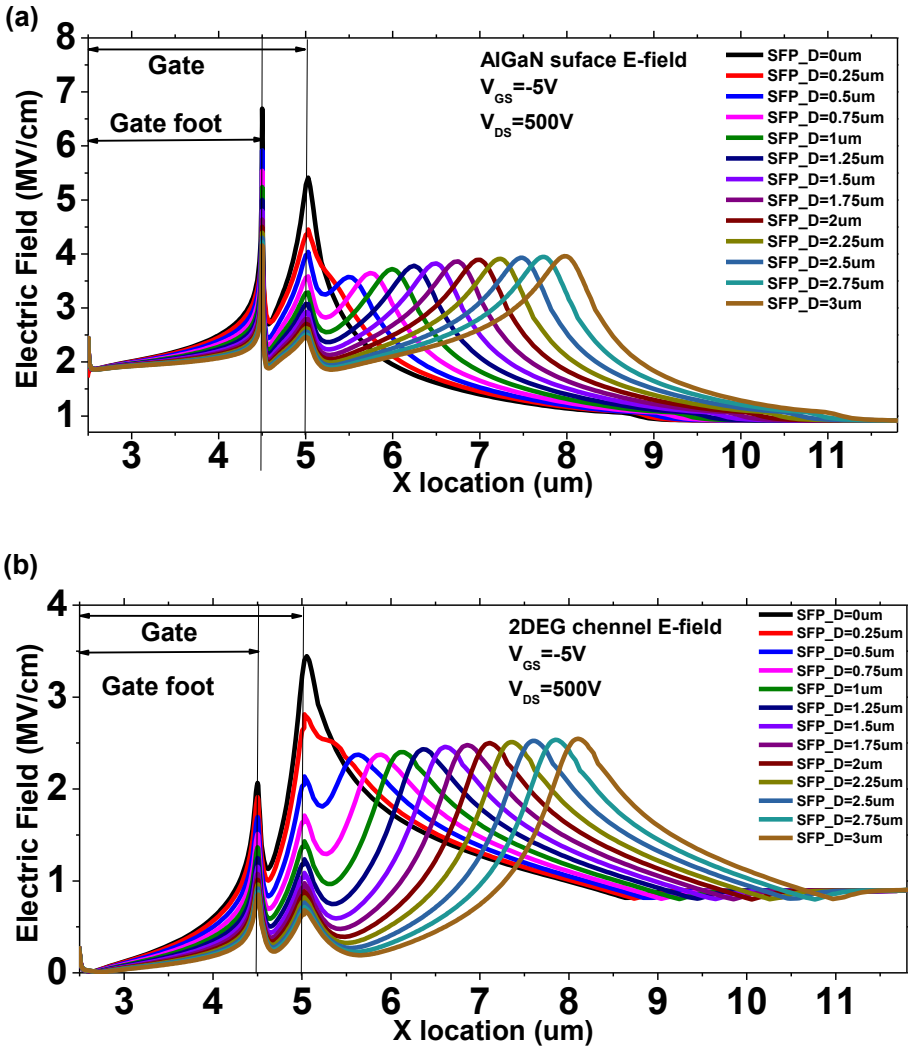

Figure 39. The simulated electric field distribution at (a) AlGaN surface (b) 2DEG channel of AlGaN/AlN/GaN HFETs with different source-field plate length (SFP_D) when V_{GS}=-5V and V_{DS}=500V.

3.4 Epitaxial layer structure

In this study, two III-N HFETs wafers with different barrier layer materials (AlGaN and InAlN) grown on different substrates were used to study the recessed-gate structure and evaluate the device performance. The epitaxy layer structures of both wafers are listed in Table 11. The $Al_{0.25}Ga_{0.75}N$/AlN/GaN HFET wafer was acquired from a commercial epitaxy vendor. The $Al_{0.25}Ga_{0.75}N$/AlN/GaN HFET structure consists of a 30nm $Al_{0.25}Ga_{0.75}N$ barrier layer, a 1nm AlN layer and a 3μm GaN buffer layer grown on a 3-inch silicon substrate (wafer ID: INTS110127h3). The AlN binary layer was designed to enhance the carrier density and mobility in 2DEG channel [159]. The sheet resistance is 250 Ω/□ measured by transmission-line-model (TLM) patterns. This $Al_{0.25}Ga_{0.75}N$/ AlN/GaN HFET wafer was used to develop the fabrication processes and study the recessed-gate HFETs for high-voltage applications.

The other InAlN/AlN/GaN epitaxial structure was grown on a SiC substrate by a Thomas–Swan MOCVD system in the AMDG group led by Prof. Russell D. Dupuis at Georgia Tech (wafer ID: 1-2036-2). The HFET epitaxial structures consist of 20 nm lattice-matched (LM) $In_{0.17}Al_{0.83}N$ barrier layer, a 1 nm AlN binary layer and a 3 μm Fe-doped GaN layer. The LM $In_{0.17}Al_{0.83}N$ barrier layer helps reduce the strain-induced defects and provides higher polarization than AlGaN layer to achieve higher carrier density in 2DEG channel. Therefore, a lower sheet resistance of 225 Ω/□ is measured from the TLM patterns. SiC substrate can provide better thermal conductivity and less lattice-mismatch-induced defects than silicon substrates. Therefore, InAlN/AlN/GaN HFETs were fabricated on this wafer to explore better d.c and microwave performance.

Table 11 A summary of epitaxy layer structure AlGaN/AlN/GaN and InAlN/AlN/GaN HFETs grown on silicon and SiC substrates used in this study

	AlGaN/AlN/GaN HFET (Wafer ID: INTS110127h3)		InAlN/AlN/GaN HFET (Wafer ID: 1-2036-2)	
Layer	Material	Thickness	Material	Thickness
Barrier layer	$Al_{0.25}Ga_{0.75}N$	30 nm	$In_{0.17}Al_{0.83}N$	20 nm
Binary layer	AlN	1 nm	AlN	1 nm
Buffer layer	GaN	3 μm	GaN	3 μm
Substrate	Silicon		SiC	

3.5 Fabrication process development

3.5.1 Fabrication process flow

The recessed-gate structure was developed using the AlGaN/AlN/GaN HFET wafer. For comparison, the same fabrication processes were also applied on non-recessed HFETs except the electrode-less wet etching. As shown in Figure 40 (a), the fabrication process of recessed-gate AlGaN/AlN/GaN HFETs starts from the mesa isolation using a chlorine-based dry etching in an ICP etching tool. After the mesa isolation, a PECVD SiO_2 layer is deposited and patterned by buffered oxide etchant (BOE) to serve as the electrode-less wet etching mask. A mixture solution of potassium persulfate ($K_2S_2O_8$) and potassium hydroxide (KOH) is prepared with designed concentration. After placing the sample in the solution, a 600 W helium-xenon flood-exposure system is used to shine ultraviolet light on the sample to catalyze the electrolyte without the need for additional current source during the wet etching.

After the recessed-gate etching, Si/Al/Ti/Au (125/500/300/500Å) ohmic metal is deposited by e-gun evaporation and annealed at 650C for 10 minutes to form the in-situ doped drain and source contact pads. A remote-oxygen-plasma treatment is applied on some samples prior the gate metal deposition to investigate the impact of surface plasma

treatment. Ni/Au gate electrodes are deposited using an electron-gun evaporator and patterned by lift-off technique to complete the recessed-gate HFETs. The schematic cross-section of the recessed-gate AlGaN/AlN/GaN HFET is shown in Figure 40 (b). Benzocyclobutene (BCB) layer is used to passivate the HFET samples, followed by the via-hole opening in an ICP tool. Finally, thick Ti/Au (500/10000Å) Metal-1 layer was deposited for interconnects and probe pads. The devices in this set of study have a range of gate width (W_G) from 0.3 mm to 10 mm.

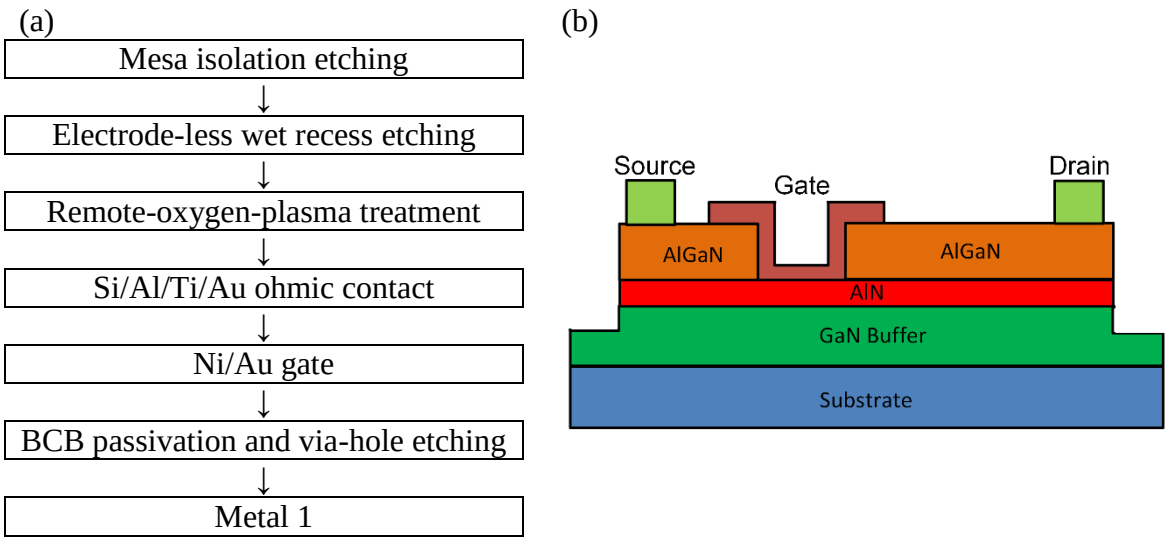

Figure 40. (a) The process flow and (b) the schematic cross section before BCB passivation for a recessed-gate AlGaN/AlN/GaN HFET.

For InAlN/AlN/GaN HFETs, similar chlorine-based dry mesa etching process is used to isolate the devices, as shown in Figure 41 (a). Ti/Al/Ti/Au metal stack (300/500/300/500Å) are patterned and annealed at 450 C for 10 minutes followed by 750C for 1 minute in nitrogen environment to achieve the specific contact resistance < 1 Ω-mm. Without a recess etching, a tri-layer e-beam lithography technique with PMMA A2/ MMA EL9/PMMA A6 resists is used to pattern the T-shaped gate. 800 μC/cm^2 and 240 μC/cm^2 doses are used to expose the gate-foot and gate-top patterns, respectively. After the e-beam lithography, Ni/Au (500/10000 Å) gate metal is deposited by e-gun

evaporation and patterned by lift-off technique. The fabricated T-gate has gate foot length of 150nm and the gate top is around 400nm wide, as shown in Figure 41 (b). The schematic of InAlN/AlN/GaN HFETs before passivation are shown in Figure 41 (c). A thick Ti/Au metal-1 layer (500/10000Å) is deposited to connect two-fingered structure with co-planer waveguide. Benzocyclobutene (BCB) layer was used to passivate the sample after the device fabrication processes.

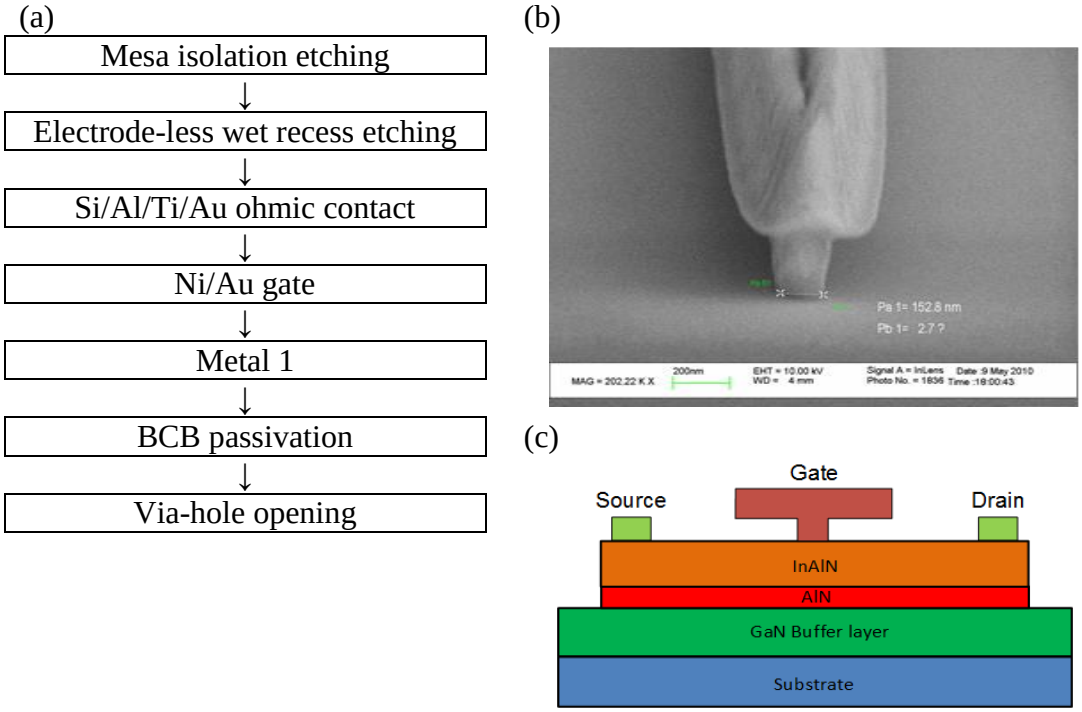

Figure 41. (a) The process flow and (b) the SEM picture of 150nm T-gate and (c) a schematic of fabricated InAlN/AlN/GaN HEMT before BCB passivation

3.5.2 In-situ doped Si/Al/Ti/Au metal scheme

For III-N HFETs, Ti/Al-based metal stacks, such as Ti/Al/Ti/Au and Ti/Al/Ni/Au, are typically used for source and drain contacts. The achievable specific contact resistance ~ 1E-5 Ω-cm^2. However, lower contact resistance is desired to improve the device performance. To address the problem, a new metal stack was studied at Georgia Tech by using a thin silicon layer in the contact metal stack as shown in Figure 42. The

additional silicon layer can create an in-situ doped *n*-type region under the metal stack which reduces the Schottky barrier thickness without using a regrowth technique. On top of the silicon layer, an aluminum layer is used to form AlN layer to reduce the Schottky barrier height. The top refractory metal layer, such as Au and Pt, are used to prevent Al and Si out-diffusion and oxidation during the post-deposition annealing. This approach helps achieve low-resistance contacts and also keeps the process simplicity of Ti/Al-based contacts. In the perspective of process integration, the Si/Al layers can also be replaced by conventional Al-Si alloy used in modern semiconductor interconnect process to further simplify the metal deposition process.

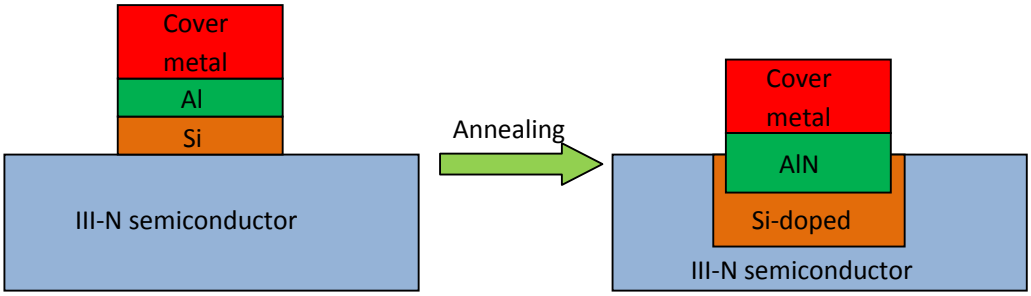

Figure 42. The schematic showing the Si/Al-based contact before and after annealing.

To validate the new metal stacks and explore the optimal process recipe, two AlGaN/AlN/GaN HFET test samples were cut from the same wafer (wafer ID: INTS110127h3) to reduce the variation from material growth. After mesa isolation etching process, 100/500/250/500 Å and 125/500/250/500 Å Si/Al/Ti/Au metal stacks were deposited separately on the two samples by e-beam evaporation and patterned by lift-off technique. Each sample was then cleaved into 9 pieces and annealed at different temperature (675,700,725 C) and time (2.5, 5, 10 minutes). Another HFET sample with 300/500/300/500 Å Ti/Al/Ti/Au metal stacks was prepared as the control sample for comparison.

In Figure 43, the contour plots of measured specific contact resistance of Si/Al/Ti/Au contacts versus the annealing time and temperature are plotted. In both figures, the lowest specific contact resistance is achieved with longer annealing time at low annealing temperature. This indicates that the Si/Al/Ti/Au stacks require proper activation energy for silicon diffusion and activation. 125 Å thick Si layer provides wider range of optimal annealing conditions than 100 Å Si layer. In Table 12, the measured specific contact resistance is reduced from 8E-6 Ω·cm for Ti/Al/Ti/Au to 3.7E-06 Ω·cm for Si/Al/Ti/Au contacts. These results demonstrate the validity of the proposed new Si/Al/Ti/Au metal stacks for the manufacture of low-resistive alloyed metal contacts. The invention disclosure regarding this novel technique has been submitted to Georgia Tech on Oct. 17, 2011 (GTRC ID: 5869.)

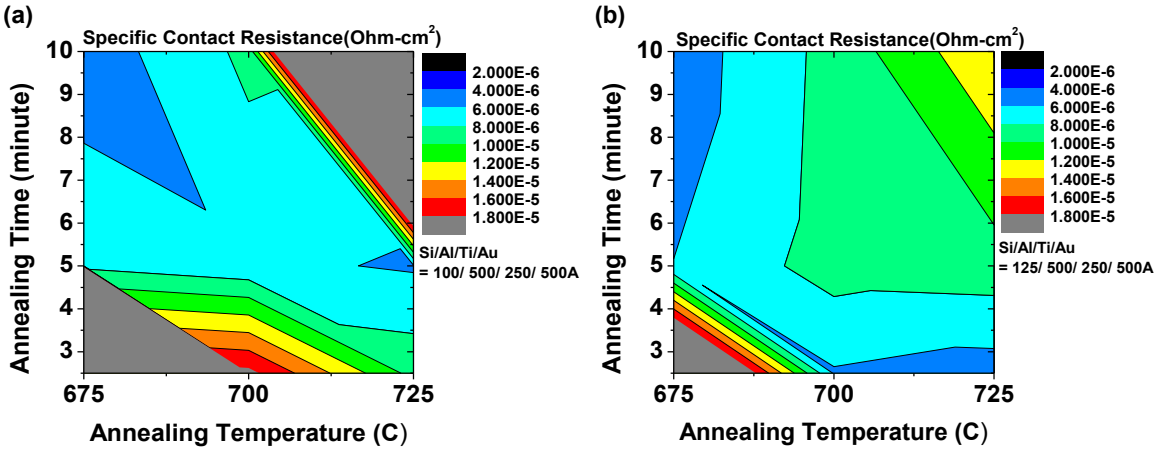

Figure 43. The contour plots of specific contact resistance of (a) 100A Si and (b) 125A Si layer of Si/Al/Ti/Au stacks versus the annealing time and temperature on HFET samples (wafer ID: INTS110127h3)

Table 12 The summary table of Si/Al/Ti/Au and Ti/Al/Ti/Au

	Annealing temperature(˚C)	Specific contact resistance (Ω·cm)	Contact resistance (Ω·mm)
Si/Al/Ti/Au (125/500/250/500Å)	675	3.7E-06	0.32
Ti/Al/Ti/Au (300/700/300/500Å)	750	8E-06	0.46

3.5.3 Electrode-less wet recess etching

To create a recessed-gate structure, plasma-enahced dry teching processes are typically used for III-N HFETs. However, the inevitable plasma deamage and the control of recess depth are very challenging. KOH-based wet etching may prevent the etching damage but the eteching unifomity is difficult to control. At Georgia Tech, a novel electrode-less wet etching was developed to create the recessed-gate structure without plasma damage. AlN layer is used as the etch-stop layer to achieve uniform recess depth and smooth etched surface across the sample.

Shown in Figure 44 is the flood exposure system used for the electrode-less wet etching process. A solution of potassium persulfate ($K_2S_2O_8$) and potassium hydroxide (KOH) with the designed concentration ($K_2S_2O_8$ = 0.001 M ; KOH = 0.002 M) is prepared as the wet etchant. The ultraviolet light generated by the 600W hellium-xenon light source is used to catalyze the electrolyte without the need for additional current source during the etching.

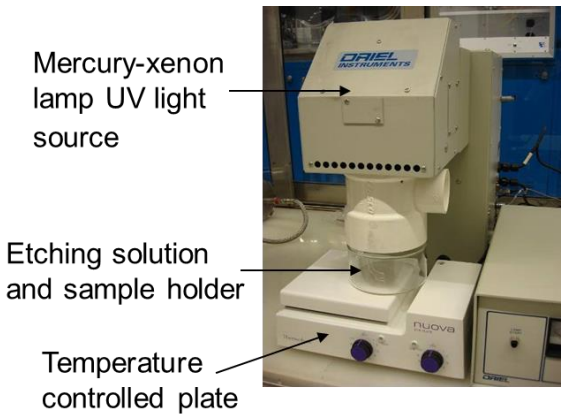

Figure 44. The flood exposure system used for the electrode-less wet etching process.

To test the wet etching rate on AlGaN layer, seven AlGaN/AlN/GaN samples were cut from the same wafer (wafer ID: INTS110127h3) and etched by the same etching process with different etching time. After removing the PECVD SiO_2 mask layer, the

recess depth was measured by an atomic-force microscopy (AFM). As shown in Figure 45, a constant etching rate of 1.1 nm/min was measured until the recess depth reached ~30 nm after 30 minutes of wet etching. After 45 minutes of wet etching, the recess depth remained unchanged. The result indicates that a high etching selectivity can be achieved between AlGaN and AlN layers in this wet-etching system. Thus the AlN binary barrier layer can be used as an etching-stop layer and the etching depth can be tightly controlled by the AlN layer in the epitaxy structure design. Because the etching-stop layer is determined by the epitaxial growth which has high uniformity across the wafer, the high uniformity of recess depth can be achieved. The stable etching rate also shows that arbitrary recessing depths can be achieved by using timed recessing etching, yielding an arbitrary threshold voltage ranging from D-mode (normally-on) to E-mode (normally-off) operations for III-N HFETs. Overall, the proposed wet-etching approach will yield robust wafer-scale manufacturability for highly integrated circuit implementation.

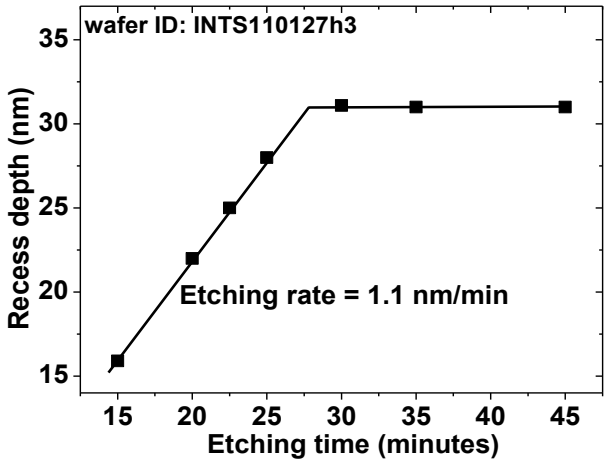

Figure 45. The recess depth versus etching time of the electrode-less wet etching process on AlGaN/AlN/GaN HFET samples (wafer ID: INTS110127h3).

The etched surface roughness was also measured by an AFM as shown in Figure 46. Compared to the as-grown surface, the roughness on the etched surface is only slightly increased from 0.255 nm to 0.37 nm. The result shows that a smooth etched

surface can be achieved using this unique wet etching approach. This novel electrode-less wet etching processes have been publish in CS MANTECH conference [160] and filed as an provision patent (US Provisional 61/552,257) by Georgia Tech Research Corporation on Oct 17, 2011(GTRC ID: 5805.)

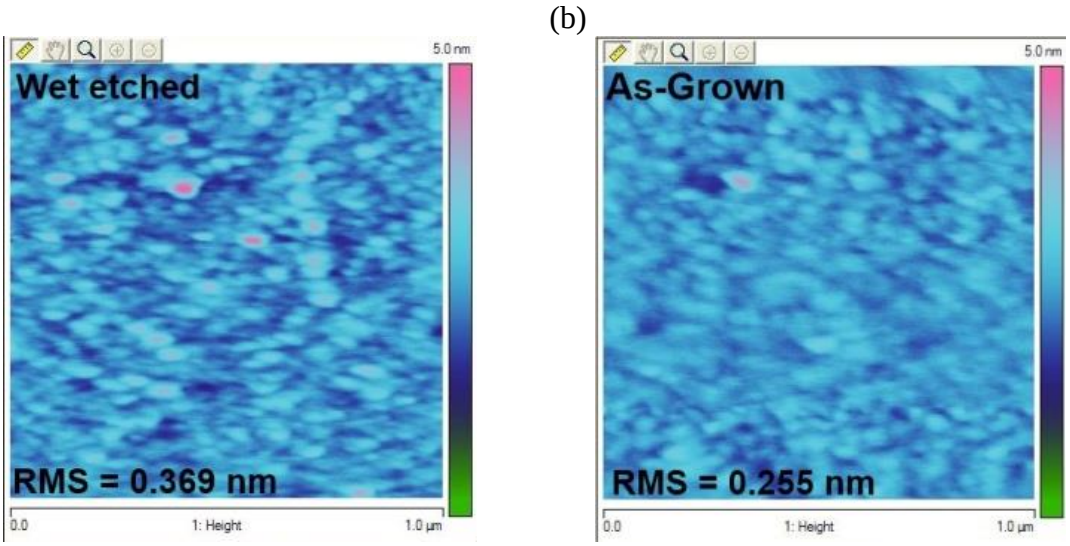

Figure 46. The atomic-force microscopy image on (a) the wet-etched surface and (b) the as-grown surface of HFET samples (wafer ID: INTS110127h3)

3.5.4 Remote-oxygen-plasma treatment

Recent studies on III-N HFETs using a gate-pulse measurement reveal that significant carrier trapping occurs near gate electrode, leading to severe current-collapse and high dynamic on-resistance. To reduce the carrier trapping in III-N HFETs, a remote-oxygen-plasma treatment in plasma-enhanced ALD (PE-ALD) tool was studied at Georgia Tech. In contrast to a PECVD system that typically excites the plasma in close proximity to the wafer surface, the PE-ALD system generates the oxygen plasma in a remote location, which is approximately 30 cm away from the main growth chamber as shown in Figure 47. Therefore, plasma damage can be eliminated in the remote-oxygen-plasma treatment.

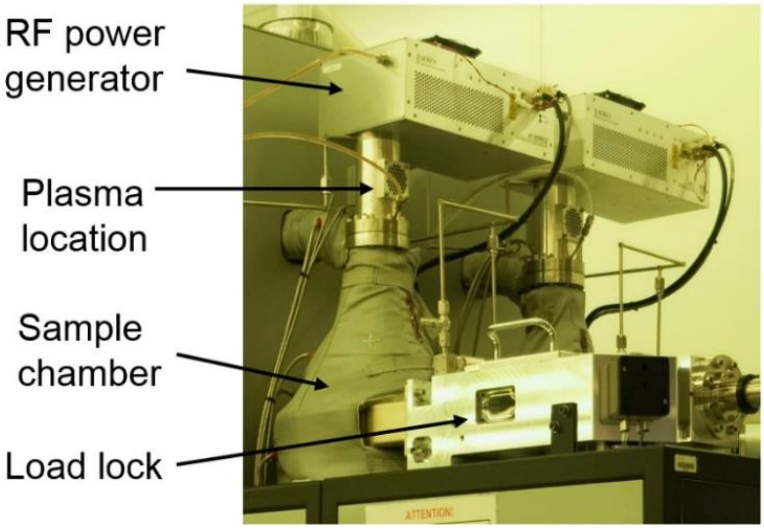

Figure 47. The Cambridge Fiji PE-ALD system used for the remote-oxygen-plasma treatment.

To evaluate the effect of the plasma treatment to the surface chemical composition before and after the plasma treatment, two samples (Sample-A and B) were cut from the same AlGaN/AlN/GaN wafer (wafer ID: INTS110127h3). After the electrode-less wet etching process to expose AlN layer on the samples, Sample-B was exposed to the remote-oxygen plasma for 3 minutes at 300C. A Thermo Scientific K-Alpha X-ray photoelectron spectroscopy (XPS) was used to measure the high-resolution XPS spectra, which can provide information on the chemical bonding in the top 5-nm surface material. Shown in Figure 48 and Figure 49 are the XPS spectra of AlGaN and AlN surfaces, respectively, on Sample-A and Sample-B. By using the Al-O (74.8 eV from Al_2O_3) and Al-N (74 eV from AlN) for the fitting of the Al_{2p} spectrum, as well as using Ga-O (21 eV from Ga_2O_3) and Ga-N (20 eV from GaN) for the Ga_{3d} spectrum [161, 162], the Gaussian-shaped fitting of these energy peaks indicate that both oxide and nitride are observed on the surfaces. For sample A without the oxygen plasma treatment, minor Al-O and Ga-O peaks (4.7 % and 9.1 %) were observed on AlGaN and AlN surface, which is due to the inevitable surface exposure to the air. After the oxygen

plasma exposure for 3 minutes on Sample-B, Al-O and Ga-O peaks on AlGaN surface are both increased to 27.9 % and 18.6 %, respectively. This indicates that the AlO and GaO are formed on the AlGaN surface while the Al-N and Ga-N peaks are still significant. The result suggests that the AlGaN surface is oxidized but the thickness of the surface oxide is much thinner than sampling depth of the XPS tool and the underlying AlGaN signals are also significant in the measured spectra.

In Figure 49. The XPS results of the exposed AlN surface show that the Al-O peak is increased from 3.3 % to 21.1 % after the oxygen-plasma treatment, while the Ga-O peak only slightly changed from 3.7 % to 5.4 %. The result indicates that the AlN layer in the recessed region is converted into $AlON_x$ but the underlying GaN buffer layer is not oxidized by the remote-oxygen-plasma treatment. Therefore, a thin layer of $AlON_x$ was formed in the recessed region of Sample-B while the unetched AlGaN region is passivated by the layer of GaO and AlO after the remote oxygen plasma treatment.

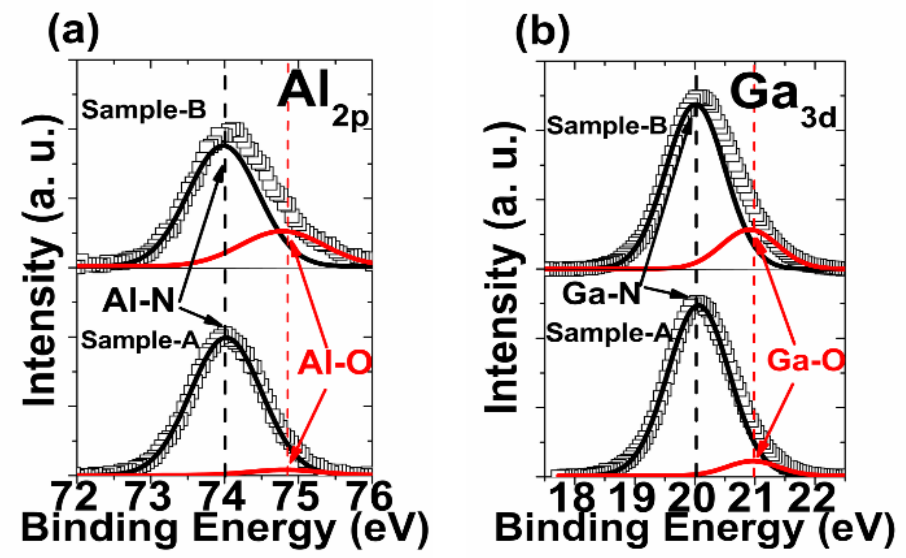

Figure 48. (a) The Al_{2p} and (b) Ga_{3d} XPS spectra of AlGaN surface on sample-A (without oxygen plasma treatment) and sample-B (with oxygen plasma treatment).

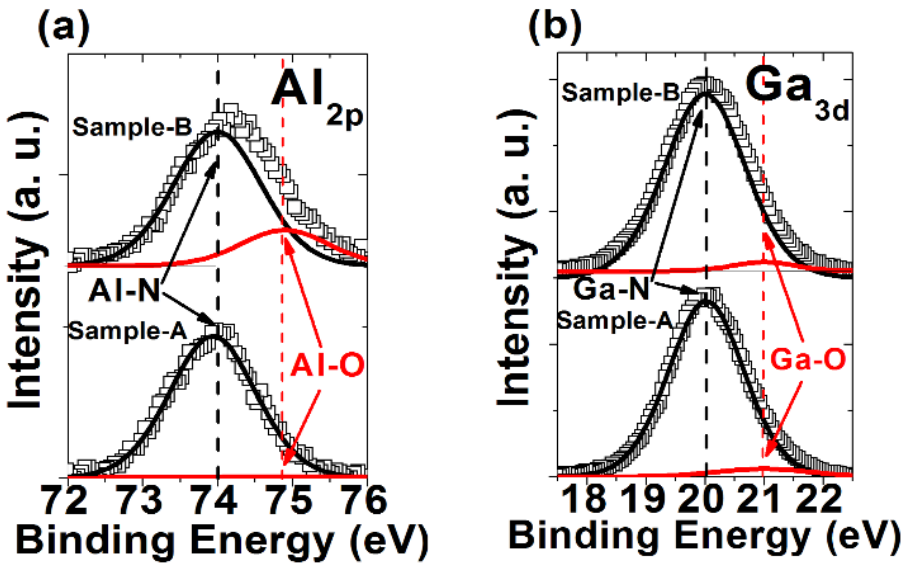

Figure 49. (a) Al_{2p} and (b) Ga_{3d} XPS spectra of AlN surface on Sample-A (without the oxygen plasma treatment) and Sample-B (with the oxygen plasma treatment).

3.6 Characteristics of AlGaN/AlN/GaN HFETs

3.6.1 Characteristics with recessed-gate structure

To study the influence of electrode-less wet recess etching to device performance, as-grown and recessed-gate AlGaN/AlN/GaN HFETs were fabricated and characterized. The measured I_D-V_{GS} curves and I_D-V_{DS} family curves of 0.3-mm-wide as-grown and recessed-gate HFETs (L_{GD} = 13 μm and L_G = 3 μm) at V_{DS} = 10 V are shown in Figure 50. The threshold voltage (V_{th}) is determined at I_{DS} = 1 mA/mm. In Figure 50 (a), V_{th} = -6 V for the as-grown HFET is shifted to 0.06 V after the recessed-gate etching. The on-off ratio is approximately identical (2×10^6) on both devices while the maximum transconductance ($g_{m,max}$) is increased from 86 mS/mm to 116 mS/mm on the recessed-gate HFET due to reduced barrier thickness. The off-state drain leakage current remains < 200 nA/mm for devices with and without the recessed-gate etching. These results confirm that good Schottky-gate properties can be achieved on recessed-gate devices. In Figure

50 (b), the I_D-V_{DS} family curves of the as-grown HFET show $I_{D,max}$ > 510 mA/mm at V_{GS} = 1V while lower $I_{D,max}$ of 420 mA/mm at V_{GS} = 4 V is observed on the recessed-gate HFETs. The specific on-resistance (R_{on}·A) of 6.6 mΩ-cm^2 on the recessed-gate HFET is also higher than 4.7 mΩ-cm^2 on the as-grown HFET. Higher on-resistance and lower maximum drain current may be attributed to the higher intrinsic channel resistance (R_{ch}) in the recess region. In Figure 51, the recessed-gate HFET with L_{GD} = 13 μm shows a breakdown voltage of 1200 V when V_{GS} = -5 V, corresponding to lateral breakdown field of 0.92 MV/cm.

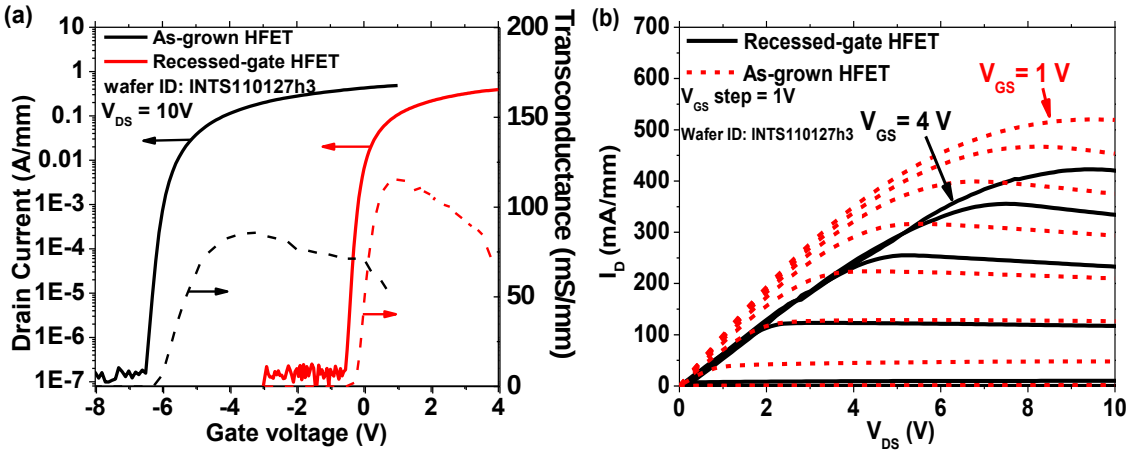

Figure 50. (a)The measured I_D-V_{GS} transfer curves and (b) I_D-V_{DS} family curves of 0.3-mm-wide HFETs with and without recessed-gate etching (wafer ID: INTS110127h3).

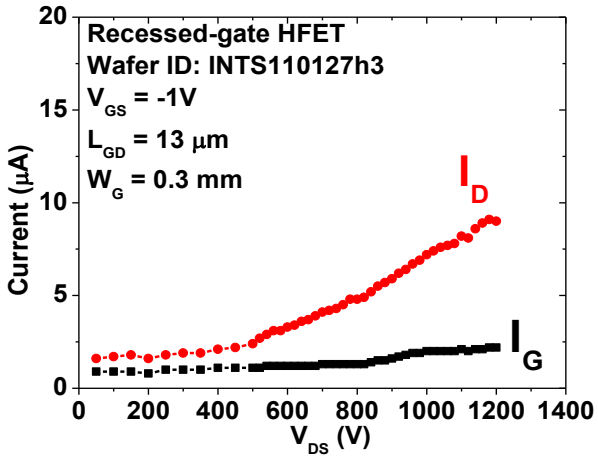

Figure 51. The drain and gate leakage current of a fabricated recessed-gate HFET (wafer ID: INTS110127h3) with W_G = 0.3 mm and L_{GD} = 13 μm at V_{DS} up to 1200V and V_{GS} = -5V.

The recessed-gate HFETs were also measured in an Agilent B1505A digital curve tracer with a pulse width of 100 μs and a duty cycle of 2 % for the maximum achievable current. Shown in Figure 52 are the family curves of a recessed-gate AlGaN/AlN/GaN HFET with W_G = 10 mm. A maximum current of 4 A, corresponding to 400 mA/mm current density, is achieved at V_{GS} = 4 V. The lower current density, when compared to 0.3-mm-wide devices, may be attributed to current spreading issue in multi-finger devices. Nevertheless, the specific on-resistance of 4 mΩ-cm^2 is measured at V_{DS} = 1 V and V_{GS} = 4 V, suggesting that the electrode-less wet etching does not cause any undesired degradation in III-N HFETs.

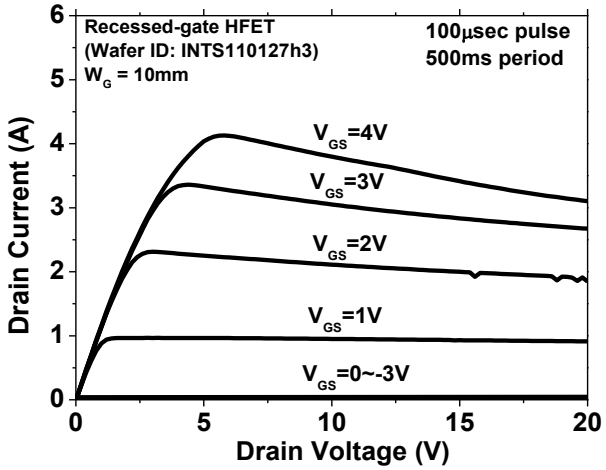

Figure 52. The on-state characteristics of a fabricated recessed-gate HFET with W_G = 10mm and L_{GD} = 13 μm.

Figure 53 shows a histogram for V_{th} distribution of fabricated HFETs with W_G = 3 mm to 10mm. The data points were collected from a wafer piece with area of 1 × 0.5 cm^2. The averaged V_{th} is -0.1 V and the standard deviation for V_{th} is 0.17 V. The relatively tight control of V_{th} suggests that uniform recess depth can be achieved with the electrode-less wet etching.

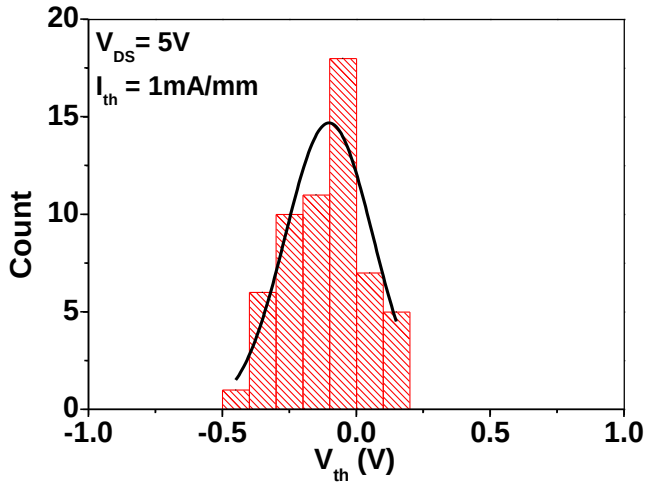

Figure 53. The histogram of measured threshold voltages of recessed-gate HFETs (wafer ID: INTS110127h3)

Figure 54 shows a device performance comparison chart for normally-off III-N FETs using different approaches. The 0.3-mm-wide recessed-gate HFET shows breakdown voltage of 1200V and $R_{on}{\cdot}A$ of 6.6 mΩ-cm^2. This corresponds to a Baliga's figure of merit (BV^2/R_{on}) of 240 MW/cm^2 which is among the state-of-the-art normally-off III-N devices.

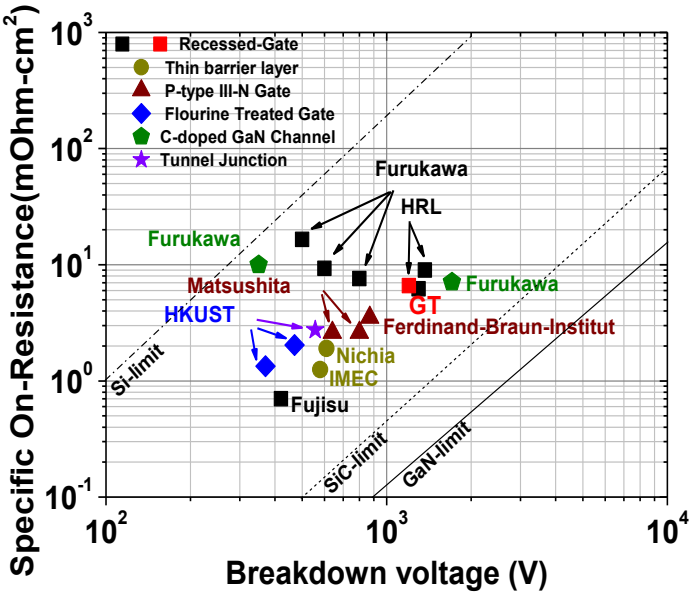

Figure 54. The specific on-resistance versus breakdown voltage for E-mode III-N high power transistors with different threshold voltage control approaches [10, 163, 164, 165, 166, 167, 168, 169, 170, 171]- [172, 173, 174]**.**

3.6.2 Characteristics with the remote-oxygen-plasma treatment

Although the recessed-gate AlGaN/AlN/GaN HFETs show good current drive and high breakdown voltage, the gate-pulse measurements revealed severe current-collapse and high dynamic on-resistance. In previous studies, these problems have been attributed to the carrier trapping near gate electrode. To improve the switching performance and to study the impact of the remote-oxygen-plasma treatment, two samples of recessed-gate AlGaN/AlN/GaN HFETs were fabricated with and without the remote-oxygen-plasma treatment. The control sample (Sample-A) and the plasma-treated sample (Sample-B) were cut from the same wafer (wafer ID: INTS110127h3). The tested devices have the same dimension (L_{GD} = 13 μm, L_G = 3 μm and L_{GS} = 2 μm). A Keithley 4200 semiconductor characterization system was used to measure d.c characteristics at room temperature. An Agilent B1505A curve tracer with single-pulse and dual-pulse setups was used to measure the quasi-static characteristics.

The measured I_D-V_{GS} transfer curves at V_{DS} = 5 V are shown in Figure 55. Compared to a recessed-gate HFETs without plasma treatment, V_{th}, defined at I_D = 1mA/mm, is shifted from -0.25 V to 0 V for a HFET that went through an additional 3 minutes of the oxygen plasma treatment prior to the gate metallization. The off-state drain leakage current is also reduced by two orders of magnitude (from 380 to 3.8 nA/mm) for $V_{GS} < V_{\text{th}}$ and an on-off ratio of 4×10^7 is achieved. The peak transconductance ($g_{m,max}$) also slightly increases from 173 mS/mm to 180 mS/mm with a broader peak-g_{m} plateau. The V_{th} shifting and significant gate leakage current suppression can be attributed to the formation of $AlON_x$ on the exposed AlN surface in

the recessed gate region after the plasma treatment. The sub-threshold slope (*S*) is also reduced from 85 mV/decade to 75 mV/decade after the remote oxygen plasma treatment.

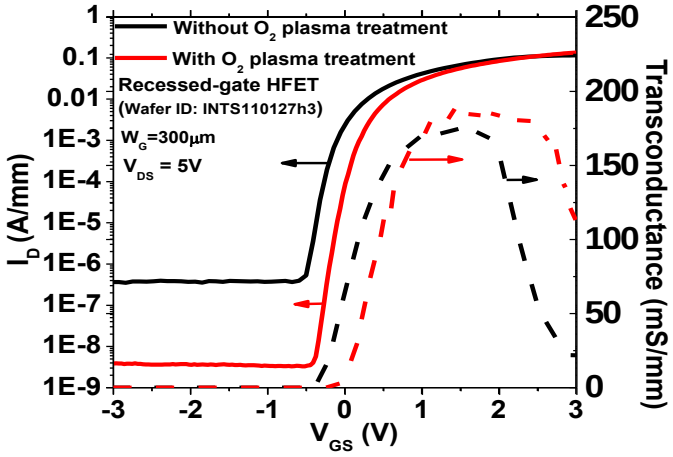

Figure 55. The measured I_D-V_{GS} curves of 0.3-mm-wide recessed-gate HFETs with L_{GD} = 13 μm and L_G = 3 μm (wafer ID: INTS110127h3) with and without the remote-oxygen-plasma treatment

The *I-V* characteristics of gate-source (GS) diodes of recessed-gate HFETs on both samples were also measured as shown in Figure 56. At low gate voltage region (-5V< V_{GS} < 2V), the GS diode for Sample-B shows lower gate leakage current than that on Sample-A. The lower leakage current is attributed to the formation of $AlON_x$ in the recessed gate region. However, the gate current (I_G) on both samples reached 1 mA/mm for V_{GS} > 3V. Therefore, the maximum V_{GS} is limited at V_{GS} = 3V on both samples.

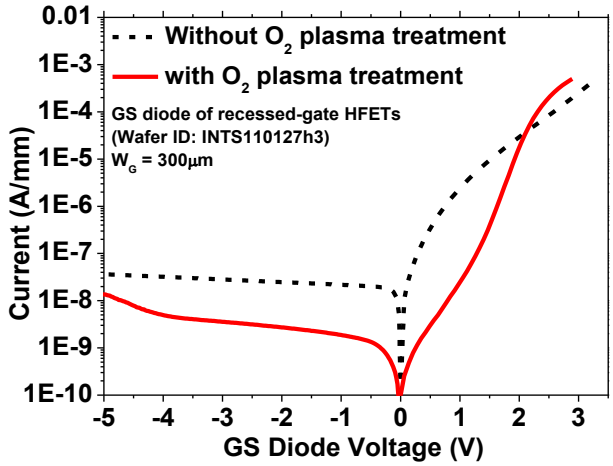

Figure 56. A comparison of the gate diode *I-V* characteristics for recessed-gate HFETs (wafer ID: INTS110127h3) with and without oxygen plasma treatment.

Shown in Figure 57 are the *C-V* curves of circular-shaped gate diodes that have a radius of 40 μm measured by a HP 4284A LCR meter with 1MHz small signal. Each *C-V* curve sweeps from -1V to 0.75V and vice versa with a sweeping time of 90 sec. The *C-V* curves show that a threshold voltage is shifted by 0.25 V after the oxygen plasma treatment, which is consistent with the shift of V_{th} from the I_D-V_{GS} transfer characteristics of recessed-gate HFETs. The hysteresis is reduced from 15 mV for Sample A to < 5 mV for Sample B. It is also noted that the slope of *C-V* curves remains the same on both samples. The two-dimensional electron gas (2DEG) carrier concentration profiles calculated from the *C-V* curves were not affected by the oxygen plasma treatment as shown in the inset of Figure 57. The *C-V* characteristics may suggest that no problematic plasma-related damage occurs during the oxygen plasma treatment, as it does not induce an increase in the interface charge density nor does it cause any change in the 2DEG redistribution in the HFET structure.

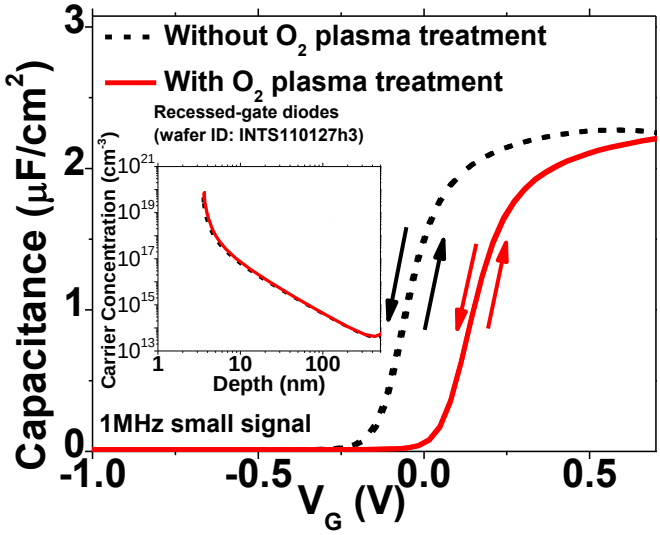

Figure 57. A set of *C-V* curves of circular-shaped gate diodes with 40 μm radius on the recessed area (wafer ID: INTS110127h3). The inset graph shows the carrier concentration profile of the diodes without and with oxygen plasma treatment

Both *d.c.* and gate-pulsed I_D-V_{DS} measurements were performed to study the influence of remote-oxygen-plasma treatment on fabricated recessed-gate HFETs. The measured *d.c.* (dotted lines) I_D-V_{DS} family curves for 0.3-mm-wide AlGaN/AlN/GaN HFETs with and without plasma treatment are shown in Figure 58. $I_{D,max}$ reaches 522 mA/mm and 465 mA/mm at V_{GS} = 3 V for devices with and without plasma treatment, respectively. To avoid the impact of I_G, the d.c. on-resistance ($R_{ON,DC}$) is evaluated at V_{GS} = 2 V and V_{DS} = 1 V. The measured $R_{ON,DC}$ are 6.8 Ω-mm and 7.1 Ω-mm for HFETs with and without plasma treatment, respectively. The maximally achievable drain current and on-resistance on HFET with plasma treatment are comparable to those on devices without plasma treatment. This indicates that the remote-oxygen-plasma treatment does not induce the current degradation and carrier depletion as reported earlier [175].

The pulsed measurement results are also shown in Figure 58 with solid line curves. The pulsed *I-V* measurement was conducted using 500-μs-wide pulses with a 50-ms period (1 % duty cycle) applied to the gate electrode. The graphs show that 32 % of drain current reduction on the HFET without plasma treatment at V_{GS} = 3V and V_{DS} = 10V while the device with plasma treatment shows 5% of increasing current due to reduced self-heating. It is shown that the remote-oxygen-plasma treatment is essentially suppressing the surface state related carrier trapping and could help improve the dynamic switching characteristics of III-N HFETs.

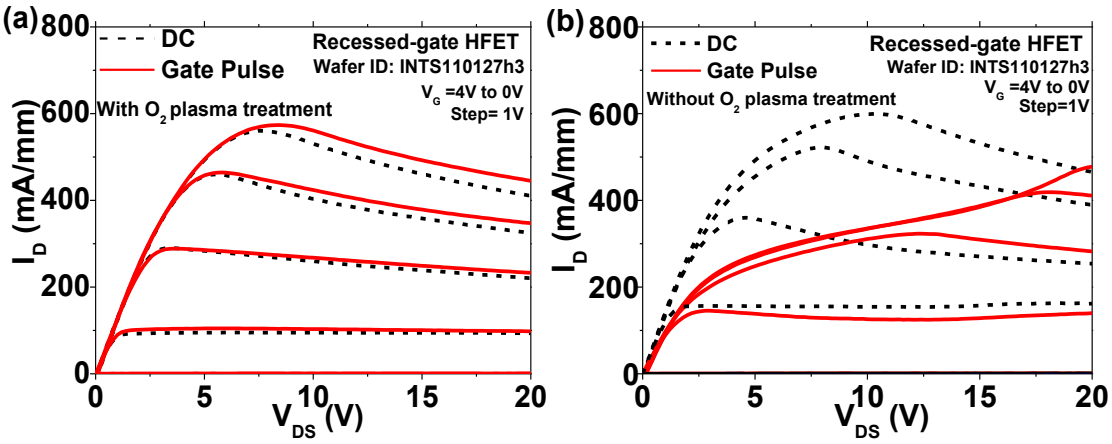

Figure 58. Measured d.c. and pulsed I_D-V_{DS} curves of 0.3-mm-wide recessed-gate HFETs (wafer ID: INTS110127h3) (a) with and (b) without remote-oxygen-plasma treatment.

The dynamic on-resistance of recessed-gate HFETs was also evaluated on both samples using a dual-pulse setup in Agilent B1505A curve tracer. The 0.3-mm-wide AlGaN/AlN/GaN HFETs on both samples were switched between the on-state (V_{GS} = 2 V and V_{DS} = 1 V) and different off-states (V_{GS} = -5 V and V_{DS} increases from 0 V to 45 V). The duty cycle was 1% (5 ms of on-state with a 500-ms period) to prevent the self-heating. The dynamic on-resistance ($R_{ON,dynamic}$) measured at V_{GS} = 2 V with V_{DS} = 1 V was compared to that evaluated in the d.c. family curve ($R_{ON,DC}$). In Figure 59, the normalized dynamic on-resistance ($R_{ON,dynamic}$ / $R_{ON,DC}$) as a function of different off-state V_{DS} values is shown. $R_{ON,dynamic}$ in Sample-A increases with the increasing off-state V_{DS} due to the off-state electron trapping under high electric field between the drain and the gate. On the other hand, the oxide formed at the surface of Sample-B helps prevent the carrier trapping, resulting in 67 % of reduction on the $R_{ON,dynamic}$ at off-state with V_{DS} = 45V. Compared to 40 % improvement using N_2O plasma treatment [176] and 80% using AlN passivation layer [177], this result demonstrates that the remote-oxygen-plasma treatment can effectively suppress the surface trap related to switching transient in AlGaN/AlN/GaN HFETs.

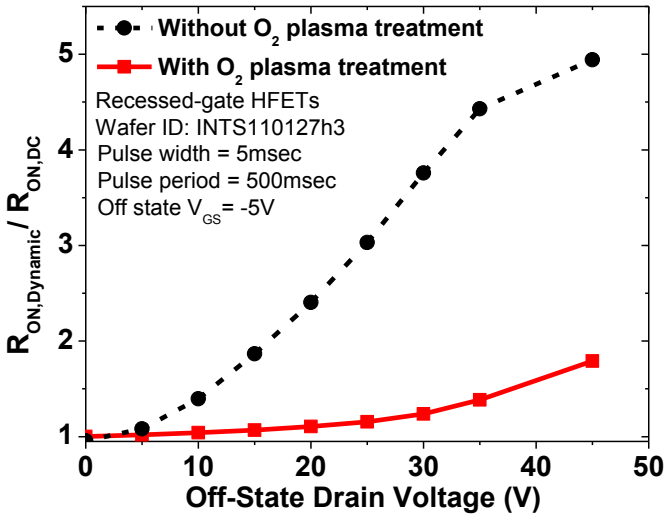

Figure 59. A plot showing the normalized dynamic on-resistance ($R_{ON,dynamic}/R_{ON,DC}$) of recessed-gate HFETs (wafer ID: INTS110127h3) with and without the remote-oxygen-plasma treatment.

3.7 Characteristics of InAlN/AlN/GaN HFETs

3.7.1 D.c characteristics

To explore better d.c and microwave performance, LM InAlN/AlN/GaN HFETs were also fabricated without a recessed-gate structure at Georgia Tech. The fabricated InAlN/AlN/GaN HFETs on SiC substrates (wafer ID: 1-2036-2) were characterized by a Keithley 4200-SCS semiconductor parameter analyzer at room temperature for d.c performance. The I_D-V_{GS} transfer characteristics at V_{DS} = 5 V and I_D-V_{DS} family curves of an InAlN/AlN/GaN HFET with gate width (W_G) = 2×25 μm are shown in Figure 60. The I_D-V_{GS} transfer curves show that the V_{th} is about -7 V and the maximum transconductance ($g_{m,max}$) reaches 250 mS/mm at V_{GS} = -4.3 V without a gate-recess structure. The $I_{D,max}$= 1.4 A/mm at V_{GS} = 1 V and V_{DS} = 10 V was achieved with the on-resistance ($R_{DS(on)}$) of 2.24 Ω·mm.

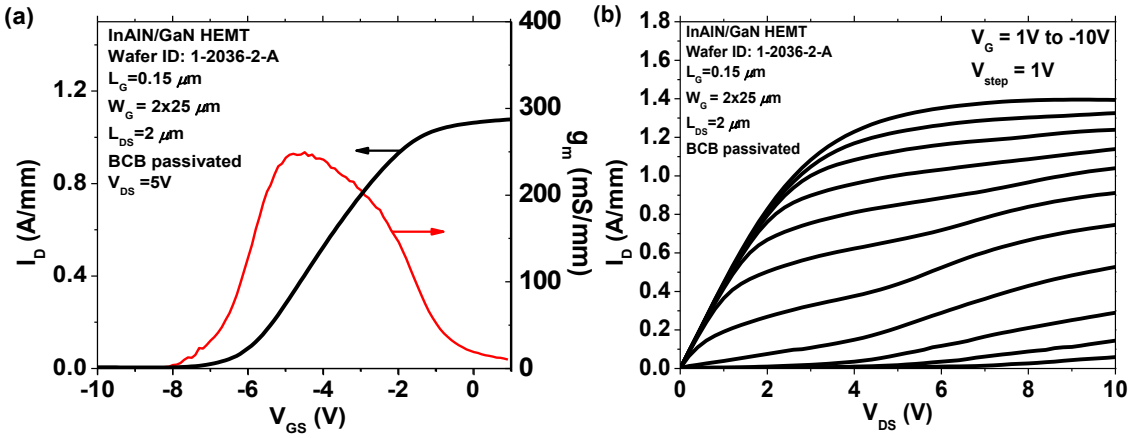

Figure 60. (a) The g_m and I_{DS} versus V_{GS} plot and (b) measured family curves of a 2×25 μm InAlN/AlN/GaN HFET (wafer ID: 1-2036-2-A) with L_G=150nm.

3.7.2 S-parameters measurements

Two InAlN/AlN/GaN HFETs with W_G = 2×25 μm and 2×50 μm were then characterized in an Anritsu 37397D Vector Network Analyzer from 40 MHz to 65 GHz at room temperature. A HP 4142B modular DC source/monitor system was used to provide d.c voltage to the bias inputs of Anritsu 37397D VNA. Before each measurement, on-wafer short-open-load-through (SOLT) calibration patterns were measured to de-embed the parasitics in the measurement system. The HFETs were measured in the common-emitter coplanar waveguide (CPW) configuration. The measured S-parameters were used to calculate the frequency-dependent $|h_{21}|^2$, *MAG* and *U* as shown in Figure 61. For 2×25-μm-wide device, a 20 dB/decade line fitting is drawn on the measured $|h_{21}|^2$ and *U* curves to determine f_T of 60 GHz and f_{max} of 188 GHz at V_{GS} = -5 V and V_{DS} = 5 V. Similarly, the 2×50-μm-wide device shows f_T = 80 GHz and f_{max} = 106 GHz at V_{GS} = -4 V and V_{DS} = 5 V. The V_{GS}-dependent f_T and f_{max} values of the 2×25 μm and 2×50 μm InAlN HFET are plotted in Figure 62. For both HFETs, f_T and f_{max} reach the maximum value at V_{GS} = -5 V where the transconductance is also highest. The

higher f_{max} for 2×50-μm-wide device is attributed to the less impact of parasitic capacitance. However, the higher gate resistance caused by longer gate finger also reduces the f_T for 2×50-μm-wide device.

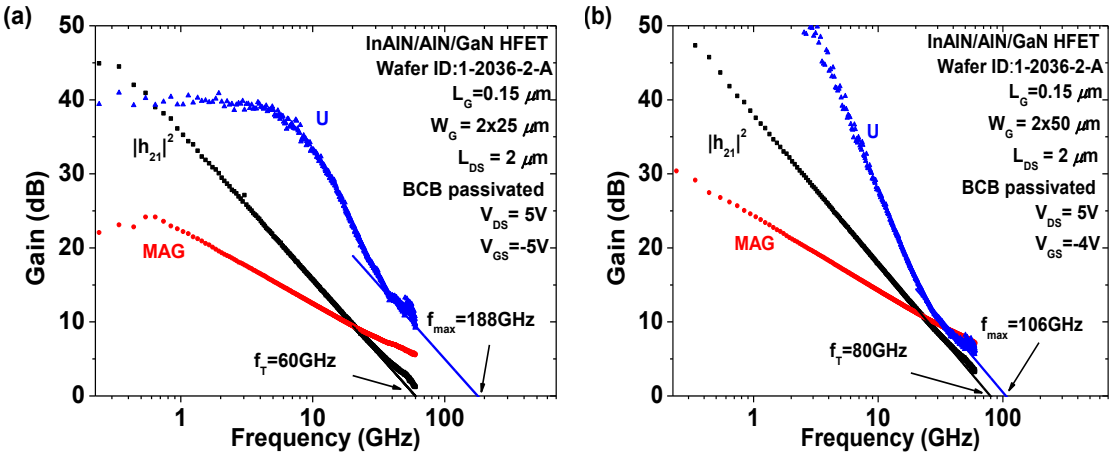

Figure 61. The frequency-dependent $|h_{21}|^2$ and U_g for (a) 2×25 μm and (b) 2×50 μm LM InAlN/AlN/GaN HFETs (wafer ID: 1-2036-2).

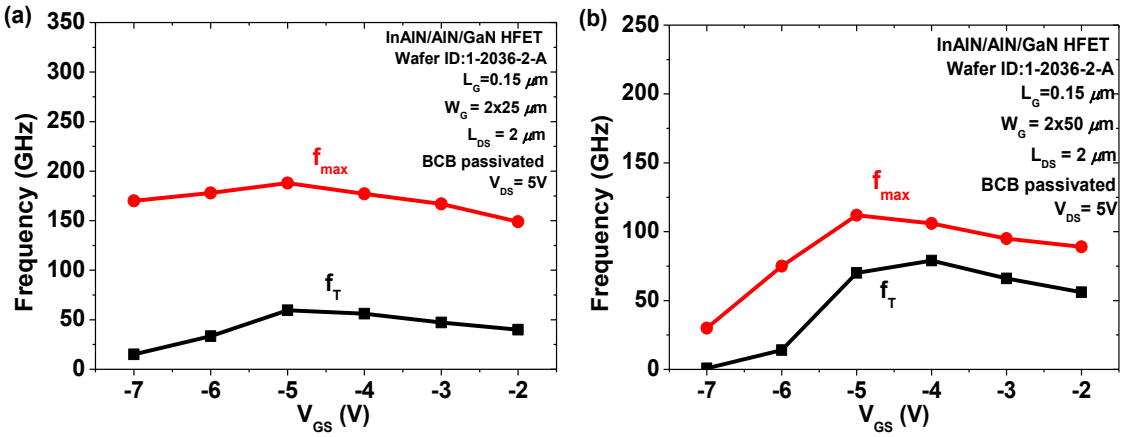

Figure 62. The corresponding f_T and f_{max} evaluation for (a) 2×25 μm and (b) 2×50 μm-wide InAlN/AlN/GaN HFETs (wafer ID: 1-2036-2-A) various gate voltages for V_{DS} = 5V.

Figure 63 shows a comparison chart for the f_T and gate length (L_G) of reported III-N HFETs. The InAlN/AlN/GaN HFET fabricated at Georgia Tech showed a f_T-L_G product of 12 GHz-μm and 9 GHz-μm for 2×50-μm and 2×25-μm HFETs, which are among the best reported microwave III-N HFETs. The results indicate that the fabrication processes are applicable to different III-N HFETs and also suggest that further

performance improvement can be achieved by more process optimization on InAlN/AlN/GaN HFETs.

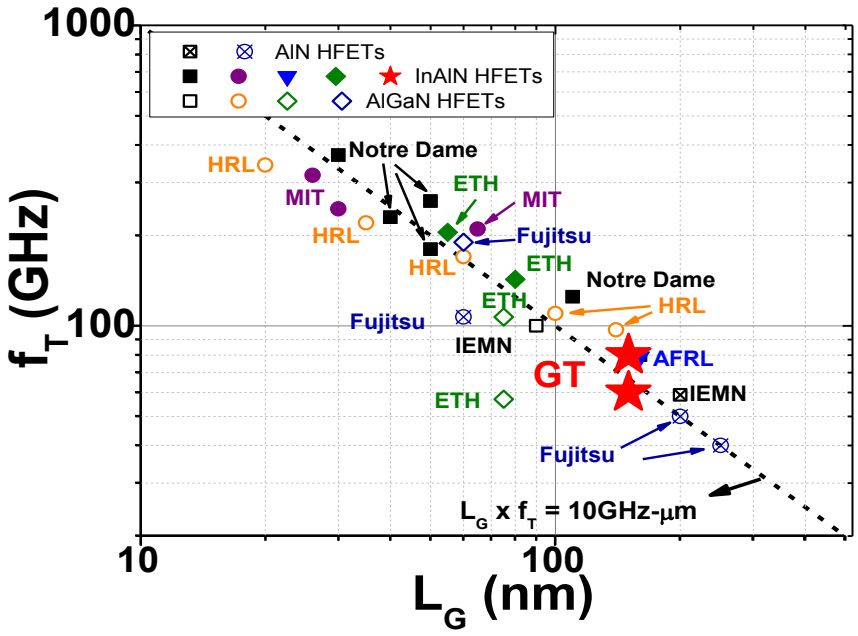

Figure 63. The cut-off frequency (f_T) versus gate length (L_G) for reported III-N HFETs [55] [56] [62] [64] [74] [178] [179] [180] [181] [182] [183] [184] [185] [186] [187] [188]

3.8 Summary

In summary, device simulation and several unique fabrication processes were developed for high-power and microwave III-N HFETs at Georgia Tech. Synopsys Sentaurus Device simulator was used to study the influence of barrier layer thickness and SFP dimension before actual device fabrication. The simulated results suggest that a recessed-gate structure is more preferable than using a thin AlGaN layer to achieve a more positive V_{th} without f_T degradation for III-N HFETs. The simulation results also indicated that 0.5~1-μm-wide SFP may be the optimal dimension to reduce the electric field in III-N HFETs for higher breakdown voltage.

Recessed-gate AlGaN/AlN/GaN HFETs were then studied experimentally using an electrode-less wet etching and a remote-oxygen plasma treatment. In-situ doped

contacts were developed to reduce contact resistance for III-N HFETs. A high etching selectivity between AlGaN and AlN was observed during the electrode-less wet etching. Uniform recess depth and smooth etched surface were achieved. The recessed-gate AlGaN/AlN/GaN HFETs show V_{th} ~ 0 V with standard deviation < 0.17 V out of 60 fabricated devices with gate width (W_G) = 3 mm to 10 mm. A maximum current drive > 4 A was achieved on a 10-mm wide recessed-gate HFET at V_{GS} = 4 V. The minimal on-resistance $R_{on}{\cdot}A$ is < 6 mΩ-cm^2 with the breakdown voltage of recessed-gate > 1200 V. It corresponds to a figure of merit (BV^2/R_{on}) of 240 MW/cm^2, which is among the best results for normally-off III-N HFETs. With the effective surface passivation by the remote-oxygen-plasma treatment, current-collapse was eliminated in recessed-gate AlGaN/AlN/GaN HFETs. The dynamic on-resistance is reduced by 67 % at off-state with V_{DS} = 45 V after the remote-oxygen-plasma treatment. The results clearly show the great potential of III-N HFETs in high-voltage and high-power switching applications.

To explore better d.c and microwave characteristics, InAlN/AlN/GaN HFETs with 150 nm-wide gate were fabricated and characterized. The highest drain current density $I_{\mathrm{D,max}}$ reached 1.4 A/mm with a maximum extrinsic transconductance ($g_{m,max}$) of 250 mS/mm. The measured on-resistance ($R_{DS(on)}$) is smaller than 2.24 Ω·mm. For 2×50-μm-wide device, f_T of 80 GHz and f_{max} of 106 GHz were demonstrated. The product of f_T and L_G for the fabricated InAlN/AlN/GaN III-N HFETs is 12GHz-μm, which is comparable to other reported III-N HFETs. These results suggest that InAlN/AlN/GaN HFETs are also promising for high-current and high-frequency applications. Based on the results in this study, three invention disclosures [189, 190, 191], three journal papers [192, 124, 193] and one conference papers [160] were published.

CHAPTER 4

DEVELOPMENT OF III-N METAL-INSULATOR-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS

4.1 Introduction

Although III-N HFETs have been demonstrated with high current drive > 400 mA/mm and breakdown voltage > 1000 V, the Schottky gate suffers from limited voltage swing and high gate leakage current. These problems can be eased by using a metal-insulator-semiconductor field-effect transistor (MISFET) structure with a high-*k* gate insulator layer. III-N MISFETs with high-*k* dielectrics deposited by different deposition techniques, such as MOCVD and PECVD, have been demonstrated [194, 195]. Al_2O_3 gate insulator deposited by atomic-layer deposition (ALD) technique is one of the promising approaches for III-N MISFETs because Al_2O_3 has better thermal stability and larger bandgap (8.8 eV) than ZrO_2 (5.7 eV) and HfO_2 (5.3 eV.) ALD deposition technique also provides a uniform deposition and more precise thickness control than other deposition techniques. However, previous studies on III-N MISFETs with ALD-Al_2O_3 gate insulator indicated that the ALD deposition recipe and the post-deposition annealing condition have significant influence on device stability and dynamic switching performance [29, 196, 197]. Nevertheless, a comprehensive study on ALD-Al_2O_3 deposition for III-N MISFETs has not yet been done because of the relatively large number of samples required for a full-scale design of experiment (DOE). In this study, to reduce the number of samples required, a 2-level fractional factorial DOE (2^{6-2} DOE) was conducted using only 16 samples to study the influence of six ALD process variables.

The results suggest that higher deposition temperature, higher annealing temperature, and longer annealing time are preferred to reduce the gate leakage current and V_{th} shifting. Higher deposition temperature, longer H_2O pulse and shorter TMA pulse help reduce the *I-V* hysteresis. With the optimal ALD deposition recipe obtained from the DOE, normally-on AlGaN/AlN/GaN MISFETs are demonstrated with ultra-low leakage current (< 1 pA/mm), small hysteresis (< 0.5 V) and high breakdown field (> 1.1 MV/cm).

Normally-off recessed-gate AlGaN/AlN/GaN MISFETs were also fabricated using the recessed-gate structure and the optimal ALD deposition recipe. The remote-plasma-treatment prior the 10-nm ALD-Al_2O_3 deposition was also applied to study the influence to device performance and trap characteristics. The plasma-treated recessed-gate MISFETs show V_{th} = 0.9 V with enhanced drain current drive (> 250 mA/mm) and transconductance ($g_{m,max}$ > 96 mS/mm) at V_{GS} = 4 V. The plasma treatment helps reduce the off-state leakage current to < 1 pA/mm, which is 2 orders-of-magnitude lower than 100 pA/mm on the MISFETs without the plasma treatment. The hysteresis and sub-threshold slope (*S*) is also reduced from 0.5 V to 0.25 V and from 110 mV/dec to 86 mV/dec, respectively, indicating the interface trap density is reduced by the plasma treatment.

To investigate the influence of plasma treatment to the traps in III-N MISFETs, frequency-dependent and light-illuminated *C-V* measurements were conducted on MIS diodes. The results from frequency-dependent *C-V* measurement suggest that the trap density (D_{it}) is reduced by 25 % to 40 % after the plasma treatment. The extracted τ is increased, suggesting that more fast traps were passivated by the plasma treatment. The

light-illuminated *C-V* measurement also shows that the density of traps are 70% lower after the remote-oxygen-plasma treatment.

To further understand the influence of plasma treatment and the trap characteristics in III-N FETs, a drain current transient analysis is performed using a similar approach described in Ref. [89]. By comparing the measurement results with other literatures using deep level transient spectroscopy (DLTS) or pulsed drain current transients on other III-N devices, the possible origin and characteristics of the traps on HFETs and MISFETs are identified. Six common traps with time constants (τ) ranging from 180 s to 3 ms are observed in HFETs and MISFETs, in addition to a trap that is peculiarly identified in the MISFETs. The results suggest that improved device performance of the plasma-treated III-N FETs is attributed to the reduced trap states with τ < 400 ms, which are located on III-N surfaces, while the slower traps (τ > 2 s) cannot be reduced by the plasma treatment and are related to the oxygen and carbon impurities and the buffer traps in the bulk semiconductors.

4.2 Device fundamentals

Similar to III-N HFETs, polarization-induced 2DEG is used as the channel for III-N MISFETs to achieve higher current drive. However, in addition to the polarization-induced electron (σ_P), the interface traps (σ_{int} in cm^{-2}) at the abrupt interface between gate insulator and III-N surface and the fixed oxide charge (N_{ox} in cm^{-3}) in the gate insulator are commonly observed in MISFETs. These additional charge have to be taken into the consideration for MIS structure. For example, the band diagram of an AlGaN/GaN MIS structure with gate oxide layer at 0 V is shown Figure 64.

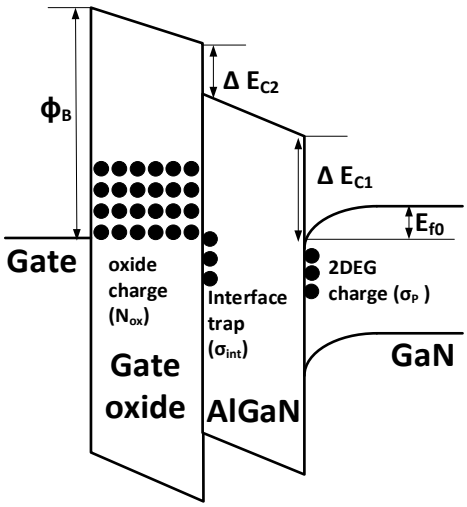

Figure 64. The band diagram of AlGaN/GaN MIS diode with a gate oxide layer at 0 V

Based on the band diagram, the V_{th} of MISFETs can be expressed as [198]:

$$V_{th,MIS} = \frac{\phi_B}{q} - \frac{(\Delta E_{C1} + \Delta E_{C2})}{q} + \frac{E_{f0}}{q} - \frac{d_{AlGaN}\varepsilon_{oxide} + d_{oxide}\varepsilon_{AlGaN}}{\varepsilon_{oxide}\varepsilon_{AlGaN}}\sigma_P - \frac{d_{oxide}}{\varepsilon_{oxide}}\left(\sigma_{\text{int}} + \frac{d_{oxide}}{2}N_{oxide}\right) \quad (41)$$

,where ϕ_B is the Schottky barrier height between the gate electrode and gate insulator. ΔE_{C1} is the conduction band offset at the AlGaN/GaN interface. ΔE_{C2} is the conduction band offset at the insulator/AlGaN interface. E_{f0} is the Fermi level with respect to the GaN conduction band. ε_{AlGaN} and ε_{oxide} are the permittivity of AlGaN and the gate oxide layer, respectively. d_{AlGaN} and d_{oxide} are the AlGaN and gate oxide thickness. σ_P is the electron density (in cm^{-2}) induced by polarization. σ_{int} is the density of charged interface traps (in cm^{-2}). Depending on the bias condition, σ_{int} can varies with time. N_{ox} is the fixed oxide charge density (in cm^{-3}) in the gate insulator layer.

According to the $V_{th,MIS}$ equation, density of interface traps (σ_{int}) has significant influence to MISFETs. To characterize the density of traps and the corresponding time constants for carrier trapping/de-trapping processes, frequency-dependent and light-

illuminated capacitance-voltage (*C-V*) measurements are commonly used on Schottky and MIS diodes.

Frequency-dependent *C-V* measurements have been previously used to investigate trap states in GaAs [199] and GaSb devices [200]. Similar approach has also been applied on III-N Schottky diodes to study the conductance dispersion related to surface and interface states in AlGaN/GaN heterojunction structure [201]. The conductance dispersion is caused by the filling and emptying of trap states. When electrons in the conduction band start to fill the trap states in the band gap, or start to be emitted from the trap states to valance band states, the energy loss causes the change of conductance. The capacitance is also affected by the trap filling or emptying process. By measuring the capacitance and conductance of an III-N Schottky or MIS diode at different frequencies, the density of traps and the characteristic time constant (τ) for trap can be estimated.

For frequency-dependent *C-V* measurements, the capacitance and conductance are measured using the equivalent parallel C_m and G_m model as shown in Figure 65 (a). A lump-element circuit is used to analyze diodes with interface traps as shown in Figure 65 (b). C_b is the gate insulator capacitance. C_s is the capacitance of the spacer layer near the heterojunction, R_s is the series resistance of the ohmic contacts. C_{it} and R_{it} are the interface trap capacitance and associated loss term for the traps. The C_{it} and R_{it} can be simplified to be G_p as shown in Figure 65 (c).

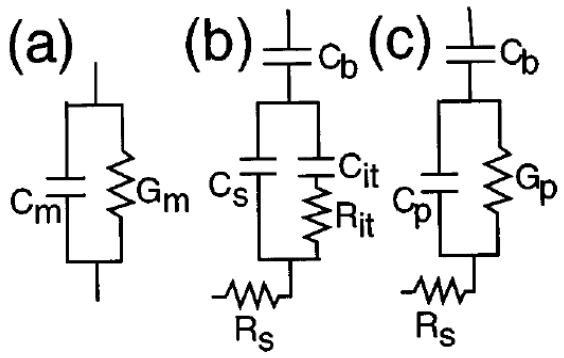

Figure 65. The equivalent lump element model used to extract trap parameters from the measured capacitance and conductance [201]**.**

Based on the lump-element models shown in Figure 65, C_p and G_p can be extracted directly from the measured C_m and G_m values using Equation (42) and (43). The R_S can be estimated from the sheet resistance and contact resistance measured from TLM patterns. C_b can be estimated from the thickness and dielectric constant of ALD Al_2O_3.

$$C_p = \frac{-C_b\left[\left(C_m^2 - C_m C_b\right)\omega^2 + G_m^2\right]}{\omega^4 C_m^2 C_b^2 R_S^2 + \omega^2\left(C_b^2 R_S^2 G_m^2 + C_m^2 + C_b^2 - 2C_b^2 R_S G_m - 2C_m C_b\right) + G_m^2} \tag{42}$$

$$\frac{G_p}{\omega} = \frac{-\omega C_b^2\left(R_S C_m^2 \omega^2 + R_S G_m^2 - G_m\right)}{\omega^4 C_m^2 C_b^2 R_S^2 + \omega^2\left(C_b^2 R_S^2 G_m^2 + C_m^2 + C_b^2 - 2C_b^2 R_S G_m - 2C_m C_b\right) + G_m^2} \tag{43}$$

Assuming the trap states form a continuous trap band, the frequency-dependent C_p and G_p/ω can be expressed as:

$$C_p = C_S + \frac{C_{it}}{\omega\tau \tan(\omega\tau)} \tag{44}$$

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau}\ln\left[1 + (\omega\tau)^2\right] \tag{45}$$

The measured G_p/ω data at different frequencies can then be fitted using Equation (45) to extract the interface trap density (D_{it}) and trap state time constant (τ). Because of the high small-signal frequency (> 20 kHz) used in *C-V* measurements, the frequency-dependent *C-V* and *G-V* can only detect the D_{it} for the traps with $\tau \sim 1$ μs with trap energy (E_{trap})

near Fermi level. For the slow traps with large time constants, the electron occupation condition of traps almost remains unchanged during the *C–V* sweeping. This means that the deep-level traps do not affect the measured *C–V* curve but act as fixed charges during the frequency-dependent *C-V* measurements.

To measure the density of traps with various energy levels, light-illuminated *C-V* measurements are proposed [196, 30]. As shown in Figure 66, under light illumination, the trapped electron with the trap activation energy level ($E_A = E_C - E_{trap}$) smaller than the photon energy ($E_{photon} = hv$) would be photo-ionized and emitted from the traps. After emitting the trapped electron, the traps become neutral or positively charged, causing the V_{th} of MIS diode shift toward negative. As a result, the shifting of measured *C-V* curves in a dark environment and a light-illuminated condition can be used to evaluate the density of traps in the MIS diodes.

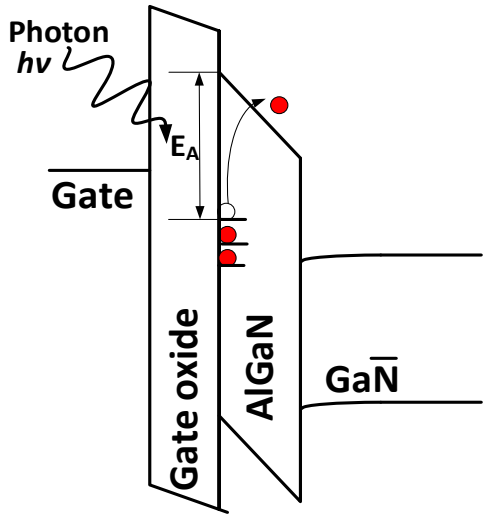

Figure 66. The schematic for photo-ionization of captured electrons under light illumination.

In addition to *C-V* measurements, drain current transient measurements are also commonly used to directly measure the characteristics of traps in HFETs and MISFETs [89, 90]. When an III-N transistor is switched from the off-state to the on-state in the

linear region, the trapped electron near the gate electrode would be de-trapped from the trap centers until a steady-state is reached. The de-trapping process is a function of the measurement time (t) and is associated with a characteristic time constant (τ) in an exponential form [202]. In some cases, a high density of traps may form a trap band instead of a single-level trap energy. A stretched exponential function is often used to model such effect [203]. The equation of the time-dependent $I_D(t)$ at linear region can be expressed as [89, 90, 203]:

$$I_D(t) = I_{D0} - \sum_i A_i \times e^{\left(\frac{-t}{\tau_i}\right)^{\beta_i}} \tag{46}$$

,where I_{D0} is the steady-state drain current. A_i represents the trap-induced current reduction depending on the density and location of traps; τ_i is the corresponding time constant for each trap level; and β_i is the stretching exponent between 0 and 1. By fitting the measured drain current transient, the time constants (τ_i) for each trap center can be extracted. For traps with similar τ on different devices, the origin and location of traps are assumed to be the same. Therefore, the values of A_i are indicative of the relative trap density in different devices with the same structure. β_i represents the spreading of trap center and may be also correlated to the traps density. For devices share the same III-N heterostructure, similar τ observed on different devices may indicate same trap states that is pertinent to the semiconductor heterostructure.

The traps can be further identified from published literatures by investigating the activation energy ($E_A = E_C - E_{trap}$.) To extract the E_A of each trap, a temperature-dependent drain transient measurement or DLTS measurements can be performed at

different temperature to extract temperature-dependent τ for each trap. For each trap, the relationship between τ and temperature T can be expressed as [204]:

$$\tau = \frac{1}{\sigma_n v_{th} N_C} \exp\left(\frac{E_C - E_T}{kT}\right) \quad (47)$$

,where σ_n is the capture cross section for electrons; v_{th} is the electron thermal velocity, which is proportional to $T^{1/2}$. N_C is the effective density of states at conduction band which is proportional to $T^{3/2}$. By plotting the measured $\ln(T^2\tau)$ against $1/kT$ in Arrhenius plots, E_A values can be extracted from the slope of linear fitting.

As summarized in Table 13, several studies using different approaches have been performed to characterize traps in III-N materials with the extracted E_A and possible origins of traps. Therefore, by comparing the E_A and τ, the possible origins of traps in fabricated III-N HFETs and MISFETs can be identified.

Table 13 The summary of traps observed in III-N devices

year	Group /University	Measure approach	Device	Time constant (@RT)	Ec-Etrap (eV)	Possible cause	Ref.
1995	NCTU, Taiwan	DLTS	Au/n-type GaN Schottky diode	30ms	0.49	carbon or the hydrogen impurities	[205]
1998	U. of Pretoria, South Africa	DLTS DLTS	Au/n-type GaN Schottky diodes	4.3s	0.78	Ion-irradiation induced N-interstitial trap	[206]
				NA	0.95	Ion-irradiation induced N-interstitial trap	
				0.3s	0.61	Defect-related traps	
2000	Wright Stale University, US	DLTS	Au/Ni/ n-GaN Schottky diodes	50s	0.89	Line defects	[207]
				55ms	0.62	Vacancies-related	
2002	Air Force Office of Scientific Research, US	DLTS	Ni/Au/n-type GaN Schottky diode	30ms	0.61	nitrogen vacancies and vacancy clusters	[208]

2002	University of Western Australia, Australia	DLTS	Ni/Au/ n-type GaN Schottky diode	NA(only seen at low T)	0.355	Mg-related defect	[209]
				400ms	0.581	Common observed traps	
2004	Nagoya University, Japan	I-DLTS	AlGaN/GaN HFET and MISFET	5ms	0.49	the damage during SiN deposition	[210]
				20ms	0.62	point-defect-related deep levels	
				10ms	0.34	AlGaN surface trap	
2004	National University of Singapore, Singapore	DLTS	Pd/Au/ n-type GaN Schottky diode	NA	0.59	defects due to dangling bonds	[211]
				NA	0.4	Silicon doping	
				NA	0.11	Nitrogen vacancy	
2005	Air Force Research Laboratory, US	C-DLTS	Ni/Au/ AlGaN/GaN Schottky diode	200s	1.02	Line defects	[87]
2008	Ohio State University, US	DLTS	AlGaN/GaN HEMTs	500ms	0.6	point defects	[212]
		DLOS		NA	1.28	carbon interstitial defect	
				NA	2.62	VGa or complexes of Vga-H	
				NA	3.28	CN substitutional defect	
2010	University of Bristol, UK	Drain current transient	AlGaN/GaN HEMTs	100s	0.45	Stressed induced C/O/H impurity defect	[213]
2010	Ohio State University, US	I_D-DLTS	AlGaN/GaN HEMTs	30ms	0.57	AlGaN surface state	[214]
		Optical DLTS		NA	1.7	carbon interstitial defect in the GaN layer	
				NA	3.76	magnesium or carbon substitutional defect in AlGaN	

2010	Slovak University of Technology, Slovakia	DLTS	Ni/Au/AlGaN/GaN Schottky diodes	NA	0.59	gallium vacancy–oxygen complex	[215]
2011	MIT, US	Drain current transient	AlGaN/GaN HEMTs	0.1	0.57	AlGaN trap	[90]
2012	Faculté des Sciences de Monastir Université de Monastir, Frence	Conductance Deep Level Transient Spectroscopy(C-DLTS)	AlGaN/GaN HEMT	300ms	0.31	AlGaN surface Electron trap	[216]
2012	MIT, US	Drain current transient	AlGaN/ GaN HEMTs	10s	0.87	NA	[217]
				0.1s	0.75	NA	
				10ms	0.57	NA	
				0.1ms	0.53	NA	
2012	Nagoya University, Japan	DLTS	Pt/Au/n-type GaN Schottky diode	NA	0.26	VN–VGa pair	[218]
				NA	0.61	NGa-related trap	
2012	Fraunhofer Institute for Applied Solid-State Physics, Germany	DLTS	AlGaN/GaN HEMTs	50s	0.44	Stressed induced C/O/H impurity trap	[219]
2013	University of Bristol, UK	Gp-ω	Fe-doped AlGaN/GaN HEMTs	NA	0.7	Fe doping	[220]
2013	Ohio State University, US	I_D-DLTS	InAlN/GaN and AlGaN/GaN HEMT	30ms	0.57	Buffer trap	[221]

4.3 Epitaxy layer structure

In this study, two AlGaN/AlN/GaN HFET structures grown on silicon and SiC substrates were used. Both wafers were acquired from the commercial epi-vendors. The

layer structures of both wafers are summarized in Table 16. For the ALD deposition study, the $Al_{0.25}Ga_{0.75}N$/AlN/GaN HFET structure grown on silicon substrate was used. The epitaxy structure consists of 30nm $Al_{0.25}Ga_{0.75}N$ barrier layer, a 2-nm AlN layer and a 4-μm carbon-doped GaN buffer layer grown on a 4-inch silicon substrate (wafer ID: NM120481-1). The sheet resistance is 300 Ω/□ measured by transmission-line-model (TLM) patterns.

For the recess-gate MISFETs and trap study, the other $Al_{0.2}Ga_{0.8}N$/AlN/GaN HFET structure grown on a 4-inch SiC substrate was used (wafer ID: GA-0633-35). The HFET epitaxial structure consists of 25-nm $Al_{0.2}Ga_{0.8}N$ barrier layer, a 1-nm AlN binary layer, a 3-μm carbon-doped GaN layer. The sheet resistance is ~ 450 Ω/□ measured by a transmission-line-model (TLM) patterns.

Table 14 A summary of layer structure AlGaN/AlN/GaN and InAlN/AlN/GaN HFETs grown on silicon and SiC substrates

	AlGaN/AlN/GaN HFET on silicon substrate (Wafer ID: NM120481-1)		AlGaN/AlN/GaN HFET on SiC substrate (Wafer ID: GA-0633-35)	
Layer	Material	Thickness	Material	Thickness
Barrier layer	$Al_{0.25}Ga_{0.75}N$	30 nm	$Al_{0.2}Ga_{0.8}N$	25 nm
Binary layer	AlN	2 nm	AlN	1 nm
Buffer layer	GaN	4 μm	GaN	3 μm
Substrate	Silicon		SiC	

4.4 Development of fabrication processes

4.4.1 Process flow

To study the impact of the process variables of ALD deposition recipes to the electrical performance of normally-on MISFETs, 16 coupon wafer pieces (~1cm × 1cm) were cut form the GaN-on-silicon wafer (NM120481-1) and processed together except

the ALD deposition and post-deposition annealing steps. The fabrication flow of normally-on AlGaN/AlN/GaN MISFETs is shown in Figure 67 (a). The fabrication processing of AlGaN/AlN/GaN MISFETs starts from the device isolation using a chlorine-based dry etching recipe in an ICP etching tool. After the device isolation, Si/Al/Ti/Au metal stacks (125/500/300/500Å) were deposited and annealed at 650 C for 10 minutes in a nitrogen environment to form the source and drain contacts.

16 different ALD deposition and post-deposition annealing recipes were then performed to deposit 15 nm Al_2O_3 layer on the coupon wafer pieces. The Al_2O_3 thickness is verified by an ellipsometer on silicon pieces deposited with the MISFET samples. The ALD deposition was performed in a home-made ALD tool (tool name: ALD2) installed at the Nanotechnology Research Center (NRC) at Georgia Tech. The post-deposition annealing is performed in an oxygen environment by an AnnealSys AS-One rapid thermal annealing (RTA) system. Finally, Ni/Au gate metal is deposited and patterned to complete the MISFETs. The fabricated MISFETs have the gate width (W_G) of 200 μm, gate-to-source distance (L_{GS}) of 1.5 μm and gate-to-drain distance (L_{GD}) of 1.5 μm. The schematic of the normally-on AlGaN/AlN/GaN MISFET structure is shown in Figure 67 (b).

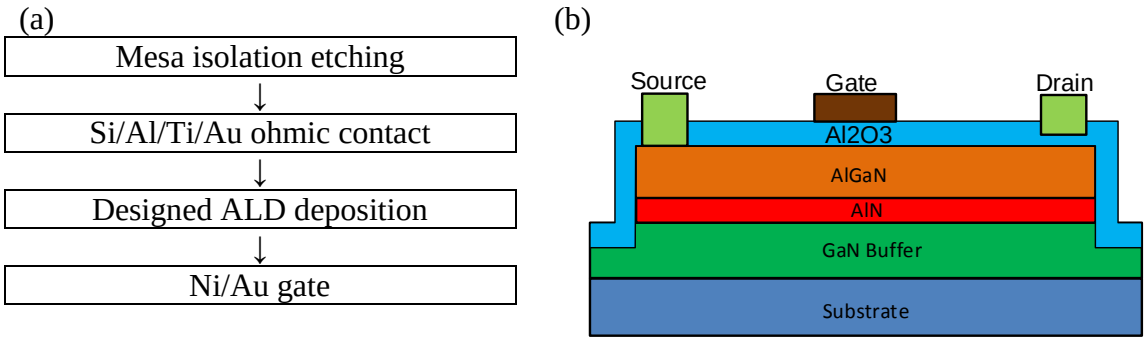

Figure 67. (a) The process flow and (b) the schematic cross section of a normally-on AlGaN/AlN/GaN MISFET.

To investigate the impact of remote-oxygen-plasma treatment and trap characteristics, two HFET samples (HFET-A and HFET-B) and two MISFET samples (MISFET-A and MISFET-B) were cut from the same GaN-on-SiC wafer (wafer ID: GA0633-35) and processed in the same batch processing run except for an additional remote-oxygen-plasma treatment applied on those "B" samples.

As shown in Figure 68 (a), the fabrication process started from an isolation etching using an inductively coupled plasma (ICP) etching tool, followed by a 30-minutes electrode-less wet etching process to create the recessed-gate area with AlN etch stop layer to achieve normally-off characteristics. The detail of the wet-etching processing technique was reported earlier [160]. After the recess etching, Si/Al/Ti/Au metal stacks (125/500/300/500Å) were deposited and annealed at 650 C for 10 minutes to form the drain and source contact pads.

After the ohmic contact step, a remote-oxygen-plasma treatment was conducted in a Cambridge Fiji PE-ALD system for both HFET-B and MISFET-B samples [192]. For the oxygen plasma treatment, 40 sccm of oxygen gas is injected into the chamber while the pressure is kept at 0.4 mTorr. The oxygen plasma exposure time was 3 minutes for HFET-B and MISFET-B. For MISFET-B, the ALD-Al_2O_3 film was deposited right after the said plasma treatment in the same growth run to prevent unnecessary surface exposure to the ambient environment. A 10nm-thick ALD-Al_2O_3 film was grown using trimethylaluminum (TMA) precursor with Ar and oxygen as the carrier gases. The growth temperature was 300 C. The ALD-Al_2O_3 deposition consists of multiple cycles of 80-ms-long TMA pulse followed by 20 seconds of oxygen plasma exposure. After the ALD deposition, the MISFET samples went through post-growth annealing in a rapid

thermal annealing system at 650 C for 7 minutes in an oxygen environment to remove $Al(OH)_x$ residue [196].

Finally, Ni/Au gate metal was deposited to complete the HFET and MISFET fabrication. The schematic device cross-sectional view for both HFETs and MISFETs is shown in Figure 68 (b).

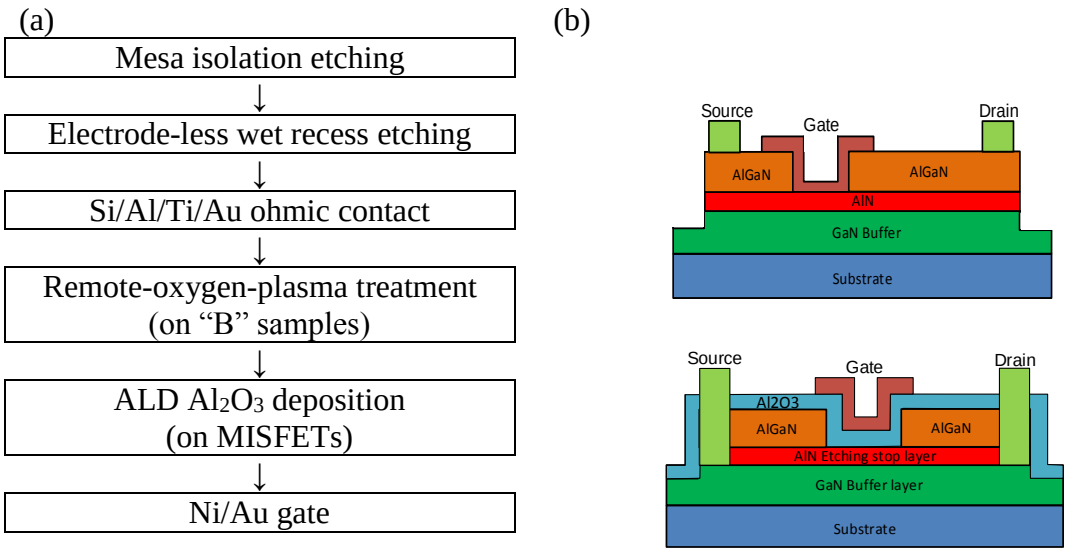

Figure 68. (a) The process flow and (b) the schematic cross-section of recessed-gate AlGaN/AlN/ GaN HFET and MISFET

4.4.2 Fractional factorial design of experiment for ALD deposition recipe

To explore the ALD Al_2O_3 deposition recipe, a home-made ALD system (ALD2) installed in the Nanotechnology Research Center (NRC) at Georgia Tech is used. The schematic diagram of the ALD system is shown in Figure 69. The system consists of two precursors, trimethylaluminum (TMA) and water (H_2O), controlled by ALD pulse valves. N_2 is used as the carrier gas in the system. All the adjustable parameters, including the deposition temperature (variable n_3), the pulse time of the TMA and H_2O precursors (variable n_4 and n_5, respectively), the gas dwelling time (n_6) as well as the post-growth

annealing temperature (n_1) and annealing time (n_2) are chosen to form the set of designed experiment.

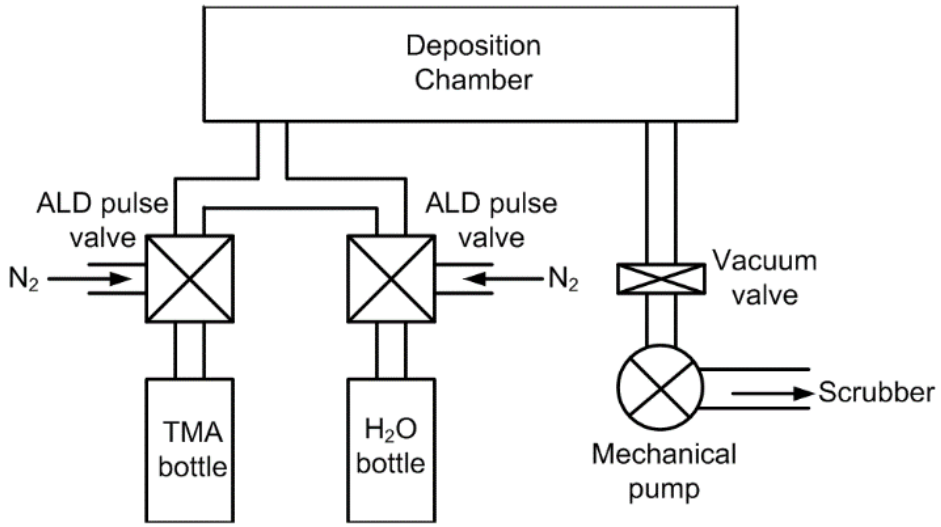

Figure 69. The schematic diagram of the ALD system (Tool name: ALD2).

A two-level experiment, i.e., the "H" and "L" states, are used for each variable designation. The actual values for "H" and "L" used for each variable are summarized in Table 15. To reduce the number of sample required, the designated levels for the TMA pulse time (n_5) and the gas dwell time (n_6) in each experiment are generated by $n_5 = n_1 \cdot n_2 \cdot n_3$ and $n_6 = n_2 \cdot n_3 \cdot n_4$. Consequently, a 2^{6-2} fractional factorial design are formed to study six variables using 16 discrete experiments. The detailed process conditions of each sample are listed in Table 16.

Table 15. The actual values used as H and L levels in in the 2^{6-2} experiment

	experimental variables [n_i]					
	Gas dwell time [n_6] (s)	TMA pulse time [n_5] (ms)	H_2O pulse time [n_4] (ms)	ALD dep. Temp. [n_3] (C)	Post-dep. Anneal Time [n_2] (min)	Post-dep. Anneal temp. [n_1] (C)
H level	5	30	50	300	7	650
L level	0	15	30	200	3	500

Table 16 A list of the assigned levels of each variable in the 2^{6-2} experiment

Sample Number (j)	experimental variables [n_i]					
	Gas dwell time [n_6]	TMA pulse time [n_5]	H_2O pulse time [n_4]	ALD dep. Temp. [n_3]	Post-dep. Anneal Time [n_2]	Post-dep. Anneal temp. [n_1]
1	L	L	L	L	L	L
2	L	H	L	L	L	H
3	H	H	L	L	H	L
4	H	L	L	L	H	H
5	H	H	L	H	L	L
6	H	L	L	H	L	H
7	L	L	L	H	H	L
8	L	H	L	H	H	H
9	H	L	H	L	L	L
10	H	H	H	L	L	H
11	L	H	H	L	H	L
12	L	L	H	L	H	H
13	L	H	H	H	L	L
14	L	L	H	H	L	H
15	H	L	H	H	H	L
16	H	H	H	H	H	H

Based on the design of experiment shown in Table 16, we can calculate the effect estimates (E_i) of each process variable and interaction (i) using the following equation:

$$E_i = \frac{\sum_j n_{ij} \times y_j}{8} \tag{48}$$

, where n_{ij} =1 at the "H" level or n_{ij} = -1 for the "L" level on the particular variables or interactions. The y_j's are the measured responses. The magnitude of the E_i represents the significance of the variable or the interaction. Larger magnitude means the variable or the interaction has more significant impact on the output response of interests. The sign of the effect estimate indicates the variable or interaction having either positive or

negative influence on the selected output when the variable or the interaction is at the "H" state.

However, because only 4 variables are fully exploited, the calculated E_i are confounded by the other variables and interactions. For example, the effect estimate of interaction $n_1 \cdot n_2 \cdot n_3$ *(E123)* is confounded by the effect estimate of n_5 *(E5)* and the interaction of $n_1 \cdot n_4 \cdot n_6$ *(E146)* because n_5 is determined by $n_1 \cdot n_2 \cdot n_3$ and n_6 is determined by $n_2 \cdot n_3 \cdot n_4$. This means that the effect estimate calculated from $n_1 \cdot n_2 \cdot n_3$ is actually a linear combination of *E5, E123* and *E126*. To simplify the result, we assume that high-order interactions are negligible when they are confounded with lower-order interactions since the variables chosen in the experiment have no obvious correlation. Thus, *E5+E123+E126*, for example, can be reduced to *E5* so the effect estimate of n_5 can be determined from the calculation of effect estimate of $n_1 \cdot n_2 \cdot n_3$.

In this study, three experiment outputs are evaluated to study the effect of each process variable. The threshold voltage (V_{th}) is determined at drain current (I_D) = 1 mA/mm to compare the V_{th} shifting (ΔV_{th}) caused by ALD-Al_2O_3 deposition. For post-ALD-growth threshold voltage shift (ΔV_{th}), we compared V_{th} with the normally-on HFET counterparts (V_{th} = -7 V) as V_{GS} sweeps from negative voltage to positive ("forward sweep") at V_{DS} = 10 V. The gate-to-source leakage current is defined by $\mathrm{Log}_{10}(I_{GS})$ at V_{GS} = V_{th} to compare the off-state gate leakage current. The *I-V* hysteresis ($\Delta V_{hysteresis}$) is defined as the V_{th} difference between the forward and the reverse sweeps at V_{DS} = 10 V. The measured experiment outputs are summarized in Table 17.

Table 17 The average values and variance of measured outputs.

Sample Number (i)	Measurement Data Summary					
	ΔV_{th} (at I_D=1mA/mm)		Log_{10} (I_{GS}) (at $V_{GS}=V_{th}$)		$\Delta V_{hysteresis}$ (V_{th} between forward and reverse sweep)	
	Avg.	Var.	Avg.	Var.	Avg.	Var.
1	-13.52	0.44	-7.03	1.78	1.57	0.003
2	-14.52	0.04	-3.96	0.03	0.33	0.013
3	-15.02	0.21	-6.37	0.65	0.6	0.13
4	-6.22	0.54	-13.1	0.02	1.03	0.003
5	-13.72	0.6	-5.17	1.27	0.07	0.003
6	-8.42	0.02	-12.3	0.01	0.6	0.01
7	-6.52	0.14	-7.4	2.47	0.07	0.006
8	-7.22	0.82	-13	0.02	0.67	0.013
9	-13.02	1.01	-4.4	0.01	0.13	0.003
10	-13.62	1.39	-6.55	0.05	0.2	0.03
11	-9.22	0.02	-5.8	1.86	0.1	0.001
12	-5.82	0.07	-12.6	0.01	0.83	0.003
13	-12.02	0.16	-6.17	0.38	0.13	0.023
14	-8.12	0.14	-6.53	1.12	0.1	0.01
15	-15.12	0.5	-5.89	0.16	0.37	0.003
16	-3.52	0.09	-6.68	0.11	0.3	0.001

In Figure 70, the plot shows that the annealing conditions (*E1* and *E2*) and ALD growth temperature (*E3*) have strong positive effect on V_{th}. The TMA pulse time (*E5*) and gas dwell time (*E6*) may slightly reduce V_{th}. However, *E5* and *E6* fall into the variance of response so they may not be statistically significant. This result suggests higher annealing temperature, longer annealing time and higher deposition temperature may be preferred for less V_{th} shift (more positive V_{th}) on MISFETs.

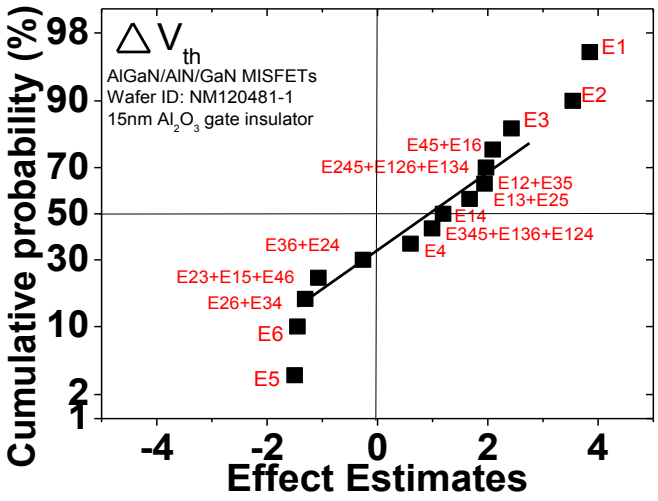

Figure 70. The effect estimates for ΔV_{th} of AlGaN/AlN/GaN MISFETs (wafer ID:NM120481-1)

In terms of the gate leakage reduction, higher temperature (*E1*), longer annealing time (*E2*) and their interaction (*E12*) shows a trend of reducing the gate leakage while longer precursor pulse time (*E5* and *E4*) may increase the leakage current, as shown in Figure 71. The statistically significant interactions are also related to *E245+E126+E134.* When the V_{th} effect is also taken into consideration, shorter TMA pulse width (negative *E5)*, longer H_2O pulses (negative *E245* and *E134*) and shorter gas dwell time (negative *E126*) could lead to reduced gate leakage current and less threshold voltage shift.

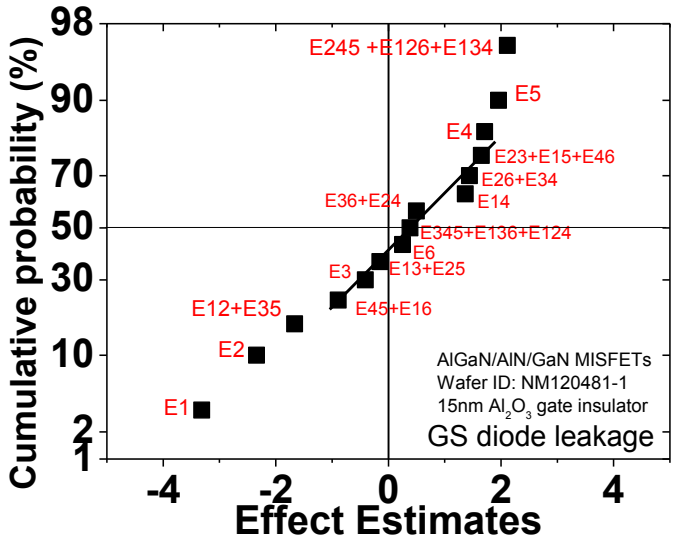

Figure 71. The effect estimates for GS diode leakage current ($Log_{10}(I_{GS})$) at $V_{GS}=V_{th}$ on AlGaN/AlN/ GaN MISFETs (wafer ID:NM120481-1)

We also determined that higher ALD growth temperature (*E3*) and longer precursor pulse time (*E4* and *E5*) may help reduce the *I-V* hysteresis of MISFETs, as shown in Figure 72. Assuming these variables also contribute to major interactions, statistically significant interactions are *E35+E12*, *E34+E26* and *E134+E126+E245*, respectively, which have opposite effect in the increase of the *I-V* hysteresis. This implied a trade-off growth condition design would exist for the precursor pulse time and the ALD deposition temperature. Combined with the analysis of V_{th} control and the gate leakage,

we conclude that shorter TMA pulse width and longer H_2O pulse width are preferred for smaller post-ALD growth V_{th} shift, low gate leakage current and lower *I-V* hysteresis.

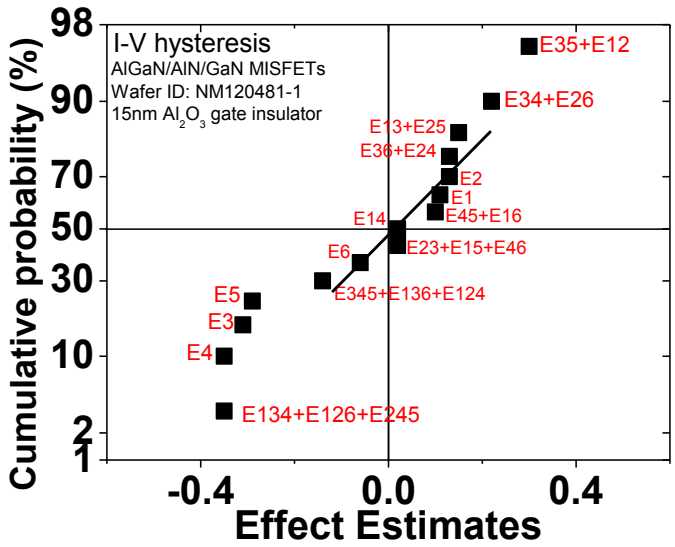

Figure 72. The effect estimates for measured *I-V* hysteresis ($\Delta V_{hysteresis}$) on AlGaN/AlN/GaN MISFETs (wafer ID:NM120481-1)

Based on this analysis, an optimal ALD deposition and annealing condition are determined with higher annealing temperature, longer annealing time, higher ALD deposition temperature, longer H_2O pulses, shorter TMA pulses and shorter gas dwell time, as summarized in Table 18.

Table 18 The optimal ALD Al_2O_3 deposition recipe

Gas dwell time [n_6] (ms)	TMA pulse time [n_5] (ms)	H_2O pulse time [n_4] (ms)	ALD dep. Temp. [n_3] (C)	Post-dep. Anneal Time [n_2] (min)	Post-dep. Anneal temp. [n_1] (C)
0	15	50	300	7	650

4.5 D.c characteristics of AlGaN/AlN/GaN MISFETs

4.5.1 Normally-on AlGaN/AlN/GaN MISFETs

The optimal ALD Al_2O_3 deposition condition was then applied to another AlGaN/AlN/GaN coupon sample (wafer ID: NM120481-1) to verify the previous findings. The measured I_D-V_{GS} transfer curves and I_D-V_{DS} family curves of the fabricated normally-on AlGaN/AlN/GaN MISFETs with a 15 nm Al_2O_3 gate insulator are shown in Figure 73. The measured ΔV_{th} is < 5 V (-7 V on HFETs to -12 V on MISFETs). *I-V* hysteresis is < 0.5 V at V_{DS} = 10 V when the gate voltage sweeps between -17 V and 0V. The off-state drain leakage current is < 1 pA/mm at V_{DS} = 10 V and a gate-to-source leakage current of < 0.5 pA/mm is measured at V_{GS} = -12 V as shown in the inset of Figure 73 (a). The family curves show I_{DSS} > 400 mA/mm with on-resistance (R_{DSon}) of 15 Ω-mm at V_{GS} = 0 V and V_{DS} = 1 V. The drain-to-source breakdown voltage (BV_{ds}) also shows > 170 V, corresponding to lateral breakdown field of 1.1 MV/cm as shown the inset of Figure 73 (b).

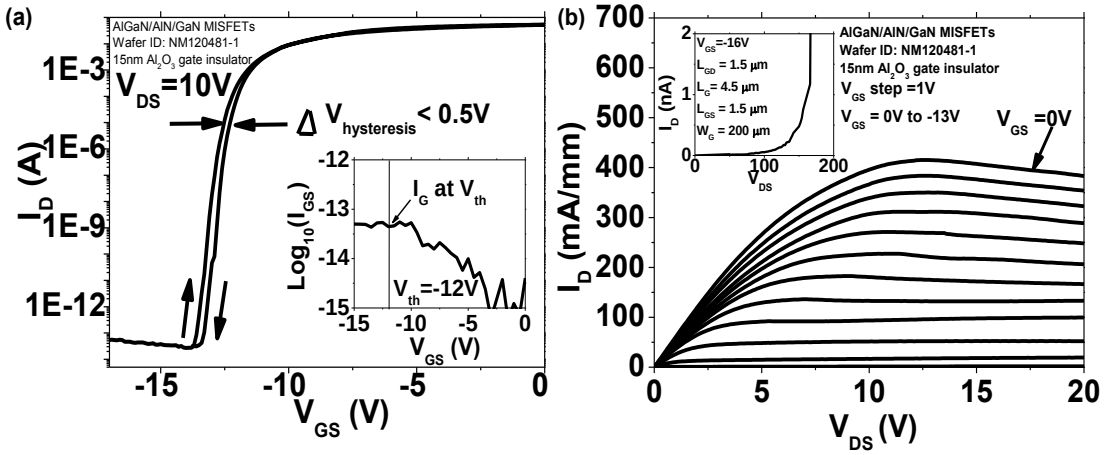

Figure 73. (a) The forward and reverse sweep of transfer curves and (b) the I_D-V_{DS} family curves and breakdown voltage of a MISFET with W_G = 200 μm and L_{GD} = L_{GS} = 1.5 μm (wafer ID: NM120481-1)

4.5.2 Normally-off Recessed-gate AlGaN/AlN/GaN HFETs and MISFETs

Although normally-on MISFETs with Al_2O_3 gate insulator demonstrate low leakage current and high breakdown field, recessed-gate MISFETs are still preferred for a normally-off operation. Using the electrode-less wet etching, recessed-gate AlGaN/AlN/GaN MISFETs were fabricated with the optimal ALD-Al_2O_3 deposition recipe. To study the influence of remote-oxygen-plasma treatment on MISFETs, two samples (MISFET-A and MISFET-B) were processed together except the remote-oxygen-plasma treatment. For a comparison study, recessed-gate HFETs (HFET-A and HFET-B) were also processed except for the ALD-Al_2O_3 deposition. An additional 3 minutes of oxygen-plasma treatment was applied on the B-samples in a PE-ALD system.

The *I-V* characteristics of recessed-gate AlGaN/AlN/GaN HFETs and MISFETs were measured in a Keithley 4200-SCS semiconductor parameter analyzer at room temperature. The devices under test have a gate width (W_G) of 0.3 mm. The gate-to-drain distance (L_{GD}) is 7.5 μm and gate-to-source distance (L_{GS}) is 2 μm. The recessed region is 1.5 μm and gate length (L_G) is 3 μm.

Shown in Figure 74 and Figure 75 are the I_D-V_{GS} transfer curves of HFETs and MISFETs at V_{DS} = 10 V. V_{GS} was swept from -1 to 3 V for HFETs and -1 to 4 V for MISFETs, respectively and the measured device characteristics are summarized in Table 19. Both HFETs and MISFETs show an increase of maximum I_{DS} by 20 % and 37 %, respectively, after the plasma treatment. The peak transconductance ($g_{m,max}$) also shows an improvement by 23 % for HFETs and 20 % for MISFETs after the plasma treatment. V_{th} is found reduced by 0.05 V and 0.1 V on the plasma-treated devices. The I_D-V_{DS} family curves of the 0.3-mm-wide AlGaN/AlN/GaN HFETs and MISFETs with and

without plasma treatment are shown in Figure 74 (b) and Figure 75 (b), respectively. With the use of plasma treatment, $I_{D,max}$ increases > 20 % at V_{GS} = 3 V for HFETs and > 25 % at V_{GS} = 4 V for MISFETs, respectively. The results indicate the remote-oxygen-plasma treatment can effectively enhance on-state characteristics for III-N FETs.

The forward and reverse I_D-V_{GS} transfer curves are shown in log scale in the insets of Figure 74(a) and Figure 75 (a). The off-state drain leakage current is reduced by more than 10 times for both HFETs and MISFETs after the plasma treatment. In addition, it was found that the gate leakage current is reduced after the plasma treatment. The reduction in the leakage current leads to high on-off ratio of 1.1E8 and 2.2E11 for HFETs and MISFETs, respectively. Compared to the typical on-off ratio of 1E8 reported for III-N MISFETs [222, 223], the result indicates an improvement of on-off ratio by more than three-orders- magnitude after the plasma treatment.

The transfer curves with forward and reverse V_{GS} sweeping directions, i.e., V_{GS} sweeping from the off to the on state versus that from the on to the off state, are also shown in the insets for evaluating the extent of the hysteresis. For samples with the additional plasma treatment, the hysteresis is reduced from 0.11 V to 0.05 V for HFETs and from 0.5 V to 0.25 V for MISFETs. The sub-threshold slope (S) is reduced also from 80 mV/decade to 75 mV/decade for HFETs and 110 mV/decade to 85 mV/decade for MISFETs, respectively. The reduced hysteresis and S suggest that the carrier trapping effects are suppressed in both HFETs and MISFETs with the remote-oxygen-plasma treatment.

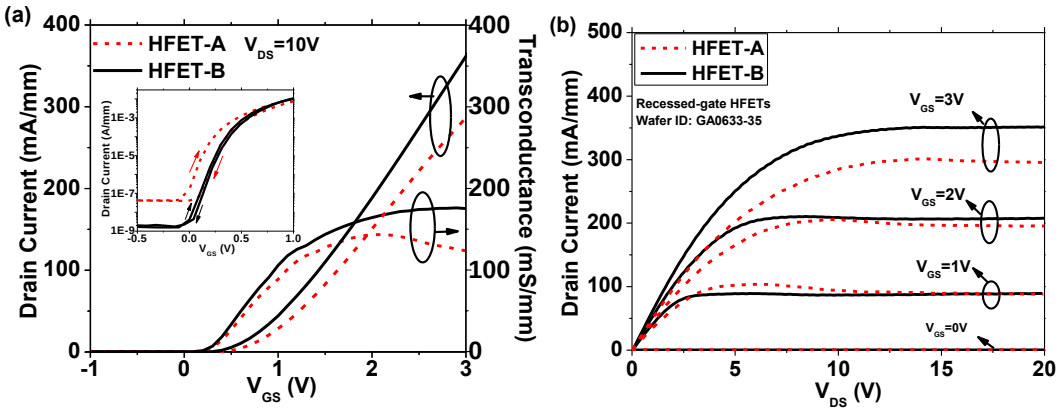

Figure 74. (a) I_D-V_{GS} transfer curves and (b) I_D-V_{DS} family curves of a 0.3-mm-wide HFET (wafer ID: GA0633-35) with and without oxygen plasma treatment.

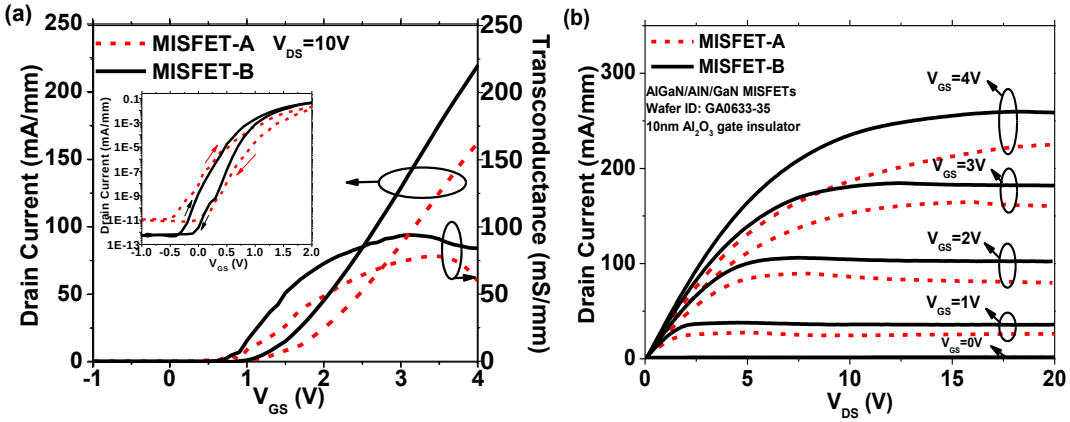

Figure 75. (a) I_D-V_{GS} transfer curves and (b) I_D-V_{DS} family curves of a 0.3-mm-wide MISFET (wafer ID: GA0633-35) with and without oxygen plasma treatment.

Table 19 The summary of device performance

	HFET-A	HFET-B	MISFET-A	MISFET-B
V_{th} (V) (at I_{DS} = 1mA/mm)	0.45	0.4	1	0.9
$g_{m,max}$ (mS/mm)	143	176	80	96
Max. I_{DS} (mA/mm)	290	350	160	220
Off-state I_{DS} (A/mm) (at V_{GS} = -1V)	< 100 n	< 3 n	< 60 p	< 1 p
I_G (A/mm) (at V_{GS}=-4V)	< 70 n	< 2 n	< 40 p	< 0.7 p
On-off ratio	> 2.9E6	> 1.1E8	> 2.6E9	> 2.2E11
Hysteresis (V)	< 0.11	< 0.05	< 0.5	< 0.25
S (mV/dec)	< 80	< 75	< 110	< 85

4.6 Trap characteristics of III-N MISFETs and HFETs

4.6.1 Frequency-dependent C-V measurements on MIS diodes

The enhanced device performance on plasma-treated HFETs and MISFETs indicates that carrier trapping is suppressed using the remote-oxygen-plasma treatment. To further understand the influence of plasma treatment to traps in III-N devices, frequency-dependent *C-V* measurements were evaluated on the MIS diodes fabricated on MISFET-A and MISFET-B samples. HP 4284A LCR meter with small signals from 1 MHz to 25 kHz was used to measure the fabricated circular-shaped recessed-gate MIS diodes with 40 μm radius on MISFET-A and B samples. The measured C_m-V and G_m-V data were measured above the threshold voltage to eliminate the effect from the buffer traps. The capacitance of Al_2O_3 layer can be estimated from the thickness and dielectric constant of Al_2O_3 ($C_b=\varepsilon_{Al2O3}/d_{Al2O3}$~0.85 μF/cm^2). The series resistance (R_S ~ 40 Ω) is estimated from the sheet resistance measured from TLM patterns. The measured C_m and G_m are used to calculate G_p/ω and plotted against the small-signal frequency ($\omega = 2\pi f$) as shown in Figure 76. Assuming that different traps comprise a continuum of levels within the bandgap, the D_{it} and τ can be extracted by fitting the G_p/ω values using Equation (45).

The extracted D_{it} and τ are plotted against V_{GS} in Figure 77. It can be seen that MISFET-B (red solid lines) has 25 to 40% lower D_{it} than MISFET-A (black dashed lines). The reduced D_{it} values on MISFET-B indicates that the remote-oxygen-plasma treatment helps reduce the density of traps. Larger τ values are also observed on MISFET-B. This may suggest that the plasma treatment passivates more fast traps with shorter τ than slower traps on MISFET-B.

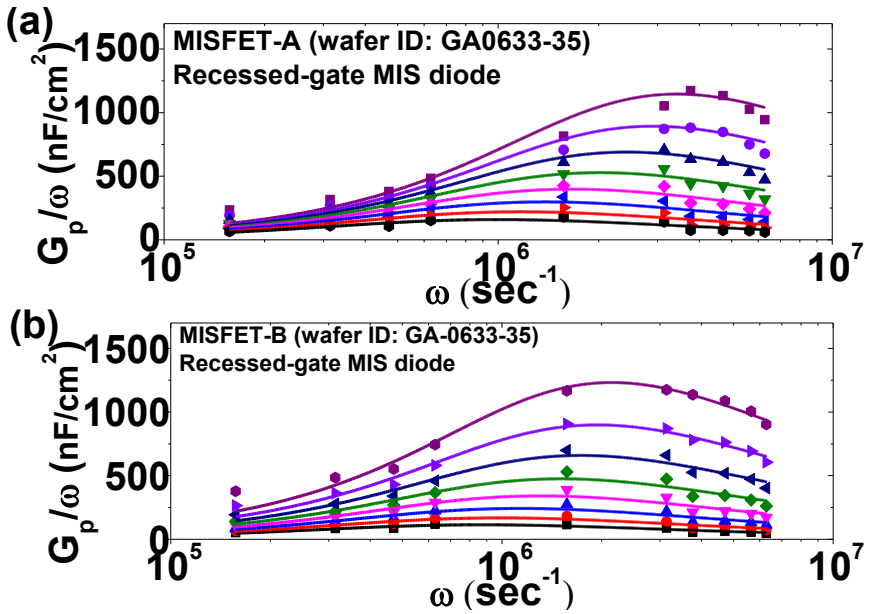

Figure 76. Frequency-dependent G_p/ω (symbols) and fitted curves on MISFET-A (without oxygen plasma treatment) and MISFET-B (with oxygen plasma treatment)

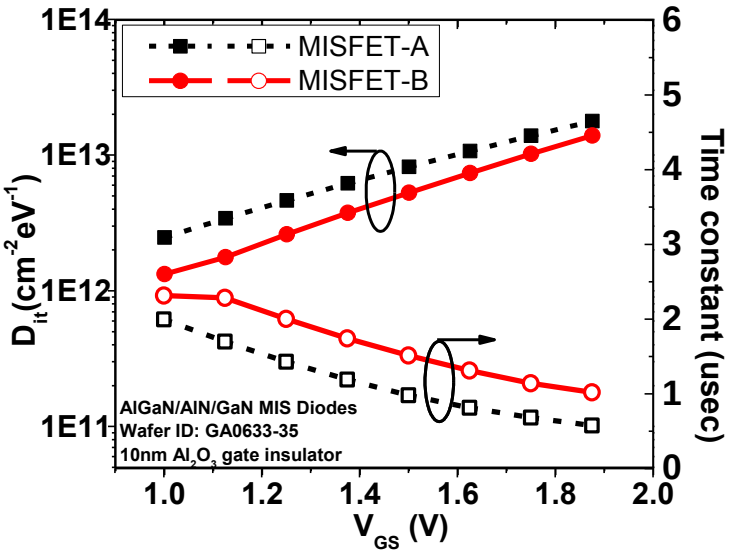

Figure 77. The fitted D_{it} and time constant τ from the MIS diodes on MISFET-A (without oxygen plasma treatment) and MISFET-B (with oxygen plasma treatment) at 1V< V_{GS} < 1.9V

4.6.2 Light-illuminated C-V measurements on MIS diodes

Although frequency-dependent *C-V* measurement indicates that MISFET-B sample with the remote-oxygen-plasma treatment has lower trap density. However, only the traps near the Fermi level with $\tau \sim 1\mu s$ are measured. To evaluate the density of deep-

level traps, a light-illuminated *C-V* measurement is conducted using a white light source without an optical filter (λ ~ 400 to 1000 nm, corresponding to photon energy E_{photon} of 3.1 to 1.2 eV, as shown in the inset of Figure 78.) The photon energy is sufficient to ionize the electron from most of the reported trap levels [89]. To completely ionizing the electron in traps, the MIS diodes were left illuminated for 5 minutes before each light-illuminated *C-V* measurement.

The *C-V* curves of MIS diodes in a dark environment (solid lines) and under a light illumination (dashed lines) are shown in Figure 78. In the dark environment, the stretch-out of *C-V* curves on MISFET-A suggests that higher interface states exists on MISFET-A sample [224]. Under the light-illumination, the *C-V* curve of MISFET-A shifts toward negative by 1 V while only 0.3 V shifting is observed on MISFET-B. The smaller V_{th} shifting suggests that a lower trap density is achieved using the remote-oxygen-plasma treatment. Assuming that the traps are located at the same location in MIS diodes, the reduced shift between *C-V* curves suggests that Q_{trap} is reduced by 70% after the remote-oxygen-plasma treatment.

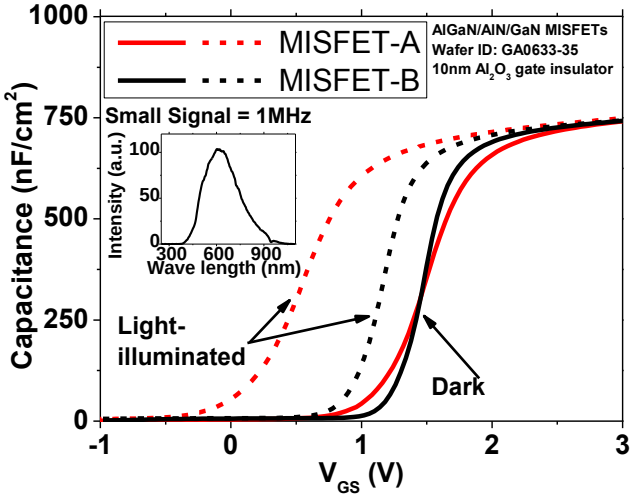

Figure 78. The C-V curves in dark environment and under light illumination measured from circular-shaped MIS diodes on MISFET-A (without oxygen plasma treatment) and MISFET-B (with oxygen plasma treatment) (wafer ID: GA-0633-35).

4.6.3 Drain current transient measurement on HFETs and MISFETs

Although *C-V* measurements confirm that the trap density is reduced after the remote-oxygen-plasma treatment, the characteristics and origins of traps cannot be resolved To further understand the influence of plasma treatment and the trap states in the fabricated III-N HFETs and MISFETs, a drain current transient analysis is performed using a similar approach described in Ref. [89].

In the drain current transient measurement, a dual-pulse measurement was performed in an Agilent B1505A curve tracer at room temperature. To prevent possible electrical-stress-induced trap generation, a shorter trap-filling time is preferred. In previous study in III-N HFETs, the trap filling time near the gate electrode is < 40 s [225]. In this study, we also found that higher off-state drain bias induces higher A_i until V_{DS} > 20 V while the extracted τ remains the same. Therefore, in the drain transient measurement setup, HFETs and MISFETs were first biased at the off-state (V_{GS} = 0 V and V_{DS} = 20 V) for 30 s to fill the traps. To prevent the self-heating, the devices under test were then switched to the linear region at V_{DS} = 1 V with V_{GS} = 2 V for HFETs and V_{GS} = 3 V for MISFETs, respectively. Lower V_{GS} is used on HFETs to prevent the gate from turning on. The measurement system is set at a sampling mode with a sampling period of 100 μs in B1505A and the measurement time (t) spans from 1 ms to 1000 s. The measured $I_D(t)$ is then normalized with I_{D0} to eliminate the variation between devices.

In Figure 79, the normalized $I_D(t)/I_{D0}$ of HFETs and MISFETs, respectively, are plotted with fitted curves using Eq. (46). $dI_D(t)/dlog(t)$ is used to determine the number of trap levels and estimate τ_i for the i^{th} trap. The estimated τ_i values are taken into Eq. (46)

to extract A_i and β_i by fitting the measured data. The sum of square error is smaller than 4E-4 for all the fitted curves. The fitted τ, A_i and β_i are summarized in Table 20 for comparison. Because HFETs and MISFETs share the same III-N heterostructure, similar τ observed on both types of devices may indicate the same origins of traps in the semiconductor heterostructure. It is found that six common traps (Trap-1 to 6) are identified in both types of devices while an additional trap (Trap-7) is observed in MISFETs.

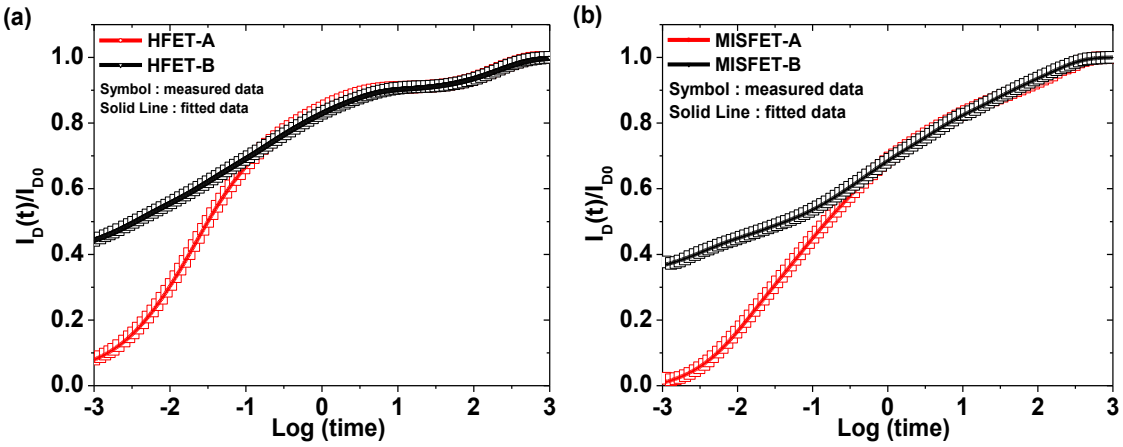

Figure 79. The normalized drain current transients ($I_D(t)/I_{D0}$) versus *log(t)* for HFET and MISFET samples. (Wafer ID: GA0633-35)

In the drain current transient plots, higher I_{DS} for plasma-treated devices is observed when compared to that on the devices without the plasma treatment at t < 100 ms. Thus the reduction of fast traps (Trap-3, 4, 5 and 6) are directly associated with the improvement in I_{DS} *and* g_m with the reduced amount of these fast traps. The slow traps (Trap-1, 2 and 7), however, cannot respond within the time frame of transfer curve measurement. In our previous study, the oxygen plasma treatment helps the formation of $AlON_x$ on the Al-rich III-N and provide effective surface trap passivation [192]. These traps are now confirmed to be fast traps with τ < 400 ms in III-N devices in the transient drain current study.

Compared to other reported results with β_i = 0.28 [203], the extracted β_i are close to 1, indicating a narrow spreading of each trap energy band in HFETs and MISFETs in this study. Nevertheless, the more stretched fitting (smaller β_i) for fast traps in HFETs may suggest that a high density of fast traps are located on the exposed III-N surfaces. On the other hand, MISFETs have all β_i > 0.99, which may suggest a lower trap density in MISFETs after the deposition of ALD-Al_2O_3 gate insulator.

Table 20. The summary of trap characteristics on HFETs and MISFETs (wafer ID: GA0633-35)

	τ	E_A (eV)	HFET-A		HFET-B		ΔA_i after plasma treatment (%)	MISFET-A		MISFET-B		ΔA_i after plasma treatment (%)	Possible origin of traps
			A_i	β	A_i	β		A_i	β	A_i	β		
Trap 1	182s	0.47	0.102	1	0.099	1	-2.94	0.137	1	0.124	1	-9.5	C/O impurity traps [205, 213]
Trap 2	2s	0.26	0.119	1	0.097	1	-18.4	0.119	0.989	0.127	1	+4.2	Buffer traps [226].
Trap 3	400 ms	0.59	0.135	0.948	0.088	1	-34.8	0.162	0.995	0.129	1	-20.3	Vacancy point defects [203, 208, 209, 212]
Trap 4	85 ms	0.3	0.226	0.964	0.104	0.949	-53.9	0.15	1	0.059	0.998	-60.6	AlGaN surface states [216, 227]
Trap 5	22 ms	NA	0.289	0.945	0.108	0.946	-62.6	0.19	1	0.049	1	-74.2	AlN surface states
Trap 6	4 ms	NA	0.095	0.947	0.088	0.947	-7.95	0.183	1	0.078	1	-57.3	Stress-induced traps [217]
Trap 7	15s	0.32	NA	NA	NA	NA	NA	0.087	0.995	0.093	0.998	+6.9	dielectric-related traps [228]

The extracted traps can be further identified from published literatures by investigating the activation energy ($E_A = E_C - E_{trap}$.) To extract the E_A of each trap, a temperature-dependent drain transient measurement was performed on all samples at

temperature from 25 °C to 125 °C. By plotting $\ln(T^2\tau)$ against $1/kT$ in the Arrhenius plot as shown in Figure 80, E_A values are extracted from the slope of the linear fitting using the data cumulated from 3 different devices of the same design. It is noted that E_A's for Trap-5 and Trap-6 cannot be determined accurately due to the measurement limitation.

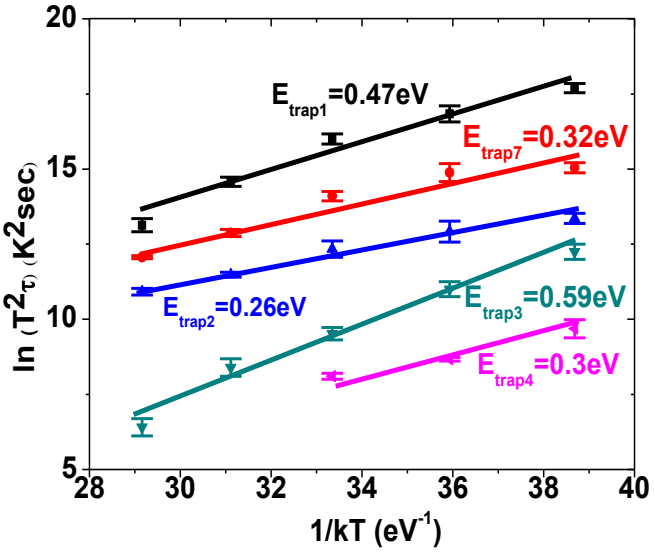

Figure 80 The Arrhenius plot of the observed traps on fabricated HFETs and MISFETs (wafer ID: GA0633-35)

By comparing the results from other reports, Trap-1 may be related to the presence of the carbon or oxygen impurities from the methyl radicals during material growth [205, 213]. Trap-2 are similar to the electron traps located in the buffer layer [226]. For Trap-3, it corresponds to the point defects related to nitrogen vacancies commonly observed in AlGaN layer [203, 208, 209, 212]. It shows less change in A_i than Trap-4 and Trap-5 after the plasma treatment. This may suggest that some point defects are located within epitaxial layer and cannot be passivated by the surface oxidation.

Trap-4 and Trap-5 show the most significant A_i reduction (> 50%) after the oxygen-plasma treatment on HFETs and MISFETs. In Ref. [216], traps similar to Trap-4 were attributed to the AlGaN surface states in AlGaN/GaN HFETs. The AlGaN surface

states have also been identified as the major cause of the current collapse [227]. Thus the reduced Trap-4 helps improve the drain current and g_m in plasma-treated devices. In this study, AlN surface was also exposed in the recessed-gate region. Therefore, Trap-5 may also be attributed to the AlN surface states which requires further study. Trap-6 has similar τ as the electrical-stress-induced traps [217]. It could be attributed to the formation of shallow traps inside AlGaN barrier. A reduction of A_i for Trap-6 is observed, suggesting that the plasma treatment also helps prevent the trap formation during the measurement.

A unique trap (Trap-7) is only observed in MISFETs. Similar A_i for Trap-7 was observed on the MISFETs with and without plasma treatment. Thus Trap-7 may be attributed to the traps in Al_2O_3 gate insulator rather than interface states [228] which is dependent on the ALD-Al_2O_3 film quality. The result indicates that the ALD deposition process could induce more slow traps in MISFETs which could affect the stability of III-N MISFETs.

Based on the results of drain current transient measurement, we may conclude that the remote-oxygen- plasma treatment helps passivate the fast traps located on III-N surfaces to achieve better device performance for both III-N HFETs and MISFET. The slow traps, however, are related to the impurities and traps in buffer layer and the gate dielectrics, which can be improved by the optimization of material growth and dielectric deposition processes.

4.7 Summary

In summary, six process variables of ALD Al_2O_3 deposition were studied for III-N MISFETs using a fractional factorial DOE. 16 samples were used to study the impact

of six ALD process variables to three electrical responses of III-N MISFETs. With the most important process variables identified, an optimal ALD deposition recipe was obtained and applied on AlGaN/AlN/GaN MISFETs. On the fabricated normally-on MISFETs, a small V_{th} shifting (< 5 V), ultra-low off-state leakage (< 1 pA/mm), and high breakdown field (> 1.1 MV/cm) were achieved. The results validate the optimal ALD Al_2O_3 deposition recipe.

To achieve normally-off operation and study the influence of plasma treatment, recessed-gate AlGaN/AlN/GaN HFETs and MISFETs were fabricated with and without the remote-oxygen-plasma treatment. With the use of plasma treatment, the drain current and transconductance are enhanced by >20% for both HFETs and MISFETs. Low off-state leakage current (< 1 pA/mm) and high on-off ratio (>1.2E11) were achieved for plasma-treated MISFETs. Smaller hysteresis and improved sub-threshold slope suggest that a lower trap density can be achieved with the plasma treatment.

To understand the influence of plasma treatment on trap characteristics of III-N devices, *C-V* measurements and drain current transient measurement were conducted on MIS diodes and transistors with and without a remote-oxygen-plasma treatment. The frequency-dependent and light-illuminated *C-V* measurements both indicate that the plasma treatment helps reduce the trap density in MIS diodes.

A drain current transient measurement was carried out to further identify the origins and characteristics of the traps. Using the stretched exponential function, six common traps are identified on the fabricated HFETs and MISFETs. One dielectric-related trap in MISFETs is also observed. The slow traps with $\tau > 2$ s are not affected by the plasma treatment and could be attributed to the carbon or oxygen impurities,

dielectric-related traps and buffer traps. The traps with $\tau < 400$ ms can be passivated by the plasma treatment, indicating that these traps are located on the exposed AlGaN and AlN surfaces in the III-N recessed-gate FETs. With the plasma treatment, the fast traps can be sufficiently suppressed, leading to an improved device performance. Based on the results in this study, one journal paper [229] and three conference papers [230, 231, 232] were published.

CHAPTER 5

SUMMARY AND FUTURE WORK

During the course of this research work, III-N transistors have been intensively studied and developed to achieve better device performance and reliability. High-voltage III-N transistors for high-power switching applications and high-frequency III-N MMICs for microwave signal amplification have been announced and commercially available. With the progress and development of III-N transistors, the market of III-N electronics is expected to grow rapidly in the next decade. However, Compared to silicon and III-V technologies, III-N transistor technology is still relatively immature due to many technical challenges in material growth and device fabrication processes. Therefore, the purpose of this research work was aimed to develop new fabrication processes and to investigate the observed issues for GaN/InGaN *npn* DG-HBTs, AlGaN/AlN/GaN HFETs and AlGaN/AlN/GaN MISFETs. The knowledge gained from the research work not only indicated the great potential of III-N transistors but also provided insights to further improvement on III-N transistor fabrication processes.

In this study, III-N *npn* DG-HBTs demonstrated promising device performance for the next-generation high-power and microwave electronic application. Compared to SiGe and III-V HBTs, III-N DG-HBTs are advantageous in high breakdown voltage, high power handling capability and high-temperature operation ability. A nitrogen-incorporated dry etching process and Pd-base *p*-type contacts were developed to enhance device performance and device stability. Different layer structures grown on sapphire and

FS-GaN substrates were studied to understand the influence of indium content and substrates to III-N *npn* DG-HBTs. A burn-in effect was studied to reduce the hydrogen-passivation in *p*-InGaN layer for III-N HBT performance enhancement. As a result, we successfully achieved state-of-the-art $h_{fe} > 110$, $J_C > 141 kA/cm^2$ and $P_{d.c} > 3$ MW/cm^2 on GaN/InGaN *npn* DG-HBTs grown on FS-GaN substrates. The high-temperature operation of InGaN HBTs up to 250 C was demonstrated. Although GaN/InGaN *npn* DG-HBTs grown on sapphire substrates suffer from higher defect density and higher junction temperature caused by poorer thermal conductivity of the substrates, we were able to successfully demonstrate high-performance III-N HBTs with $h_{fe} > 76$, $J_C > 95$ kA/cm^2 and $P_{d.c} > 1.3$ MW/cm^2. The first microwave performance of InGaN HBTs was demonstrated for devices built on a sapphire substrate. The measured device shows $f_T > 8$ GHz and $f_{max} > 1.8$ GHz. A small-signal model for III-N HBT was extracted. A study shows that the intrinsic microwave performance of the current generation of InGaN HBTs could achieve a $f_T > 39$ GHz should the contact resistance be significantly improved.

Based on the achievement on III-N HBTs in this study, the next goal of the research on the GaN/InGaN *npn* DG-HBTs may be focus on the contact resistance and further device scaling for a higher current density and cut-off frequency. Despite of the significant improvement of Pd-based contacts, the unstable Schottky *p*-type contacts and the high base resistance still prevent higher current density required for high frequency operation. Compared to InP-based HBTs with $J_C > 1 MA/cm^2$ [31, 32], the achievable J_C on III-N HBTs (> 140 kA/cm^2) are still 10 times lower. The analysis on the carrier transit time in GaN/InGaN DG-HBTs and small-signal model also indicate that the contact

resistance still dominates the f_T of DG-HBTs. High base resistance is also the cause of electromigration of *p*-type contacts in DG-HBTs due to the joule heating. To solve the problems, future work may be focused on the process improvement for *n*-type and *p*-type contacts to reduce the contact resistance. A study on Si-incorporated contacts on III-N HFETs demonstrated new opportunity to achieve lower contact resistance on *n*-type III-N semiconductors. Therefore, Si-doped and Mg-doped contact schemes may be utilized to further improve *n*-type and *p*-type contacts for III-N DG-HBTs, respectively. In addition, the Schottky *I-V* characteristics observed on the *p*-type contact suggest that dry etching damage still occurs during the mesa etching processes. Further optimization of the dry etching processes is required to eliminate the etching-induced type conversion for lower base contact resistance. The electrode-less wet-etching technique may be an alternative approach to expose the base region without plasma damage but further studies are required to achieve a uniform wet etching process.

Aggressive device scaling is also required to reduce the capacitances for higher microwave performance of III-N HBTs. Because of the limitation of optical lithography, the achievable smallest device size is limited at 3 ~ 5 μm for GaN/InGaN *npn* DG-HBTs in this study. Using more sophisticated lithography methods such as the e-beam lithography, sub-micron DG-HBTs can be implemented. The smaller device dimensions not only reduce the parasitic components but also reduce the current crowding effect caused by the high base resistance.

III-N HFETs are commercially available III-N transistor products for high-voltage and microwave applications to date. In this thesis, the Synopsys Sentaurus Device simulator was used to study the influence of epitaxy structures and recessed-gate

structure before actual device fabrication. The simulation results indicate that a more positive V_{th} can be achieved without f_T degradation by using a recessed-gate structure. A 0.5 ~1-μm-wide source-field plate is also helpful to reduce the electric field in III-N HFETs. Based on the simulation results, the fabrication technology for recessed-gate AlGaN/AlN/GaN HFETs were developed using an electrode-less wet etching and a remote-oxygen plasma treatment. Lower contact resistance (< 4E-6 Ω-cm^2) was achieved by in-situ Si-doped contacts. A high etching selectivity between AlGaN and AlN was observed using the electrode-less wet etching process to achieve uniform recess depth and smooth etched surface. The recessed-gate AlGaN/AlN/GaN HFETs show V_{th} = 0.6 V with standard deviation < 0.17 V out of 60 fabricated devices with gate width (W_G) = 3 mm to 10 mm. The minimal on-resistance $R_{on}{\cdot}A$ of 6 mΩ-cm^2 with the breakdown voltage of recessed-gate > 1200 V was achieved, corresponding to the BFoM (BV^2/R_{on}) of 240 MW/cm^2. With the remote-oxygen-plasma treatment, current-collapse in recessed-gate AlGaN/AlN/GaN HFETs was eliminated and 67% lower dynamic on-resistance was achieved. The InAlN/AlN/GaN HFETs with sub-micron gate length (L_G = 150 nm) also demonstrated f_T of 80 GHz and f_{max} of 106 GHz.

For III-N HFET development, normally-off operation, lower on-resistance and better device reliability are highly desired for successful commercialization of this device technology. Despite V_{th} of 0.6V was achieved in this study, the threshold voltage is still not high enough for actual high-voltage switching circuits to provide a direct component drop-and-replace of existing silicon power transistors due to the stringent requirements of signal noise tolerance and breakdown voltage overhead for power electronic systems. A remote-oxygen-plasma treatment with the PECVD SiO_2 wet etching mask layer may be

used for a selective surface oxidation in the recessed region since the remote-oxygen-plasma treatment has been proven effective to oxidize III-N surfaces without causing problematic plasma damage. The preliminary study also showed a 0.25 V V_{th} shifting after 3 minutes of plasma treatment. It might be expected that a longer plasma treatment time may help result in a more positive V_{th} with a lower gate leakage current.

In addition to III-N HFETs, the study on the III-N MISFETs demonstrated their potential for ultra-low-power applications. With the optimized ALD-Al_2O_3 deposition recipe obtained from the 2^{6-2} fractional factorial DOE, the fabricated AlGaN/AlN/GaN MISFET demonstrated ultra-low off-state leakage current of < 1 pA/mm and state-of-the-art on-off ratio of greater than 2.2E11. Using an electrode-less etching technique developed in this work, normally-off operation was also achieved on recessed-gate AlGaN/AlN/GaN MISFETs with V_{th} > 0.9V. The *C-V* measurements and the drain current transients indicated that the remote-oxygen-plasma treatment was effective to improve the performance of III-N MISFETs by reducing slow-trap densities. An additional dielectric-related slow trap was observed on MISFETs, suggesting that the ALD deposition process induced additional traps in MISFETs and further processing optimization on the gate dielectrics would be required.

Future III-N MISFET development may be focused on further improvement for the gate insulator deposition processes and study the dielectric-related traps using different measurement approaches. On the other hand, although Al_2O_3 gate insulator has been demonstrated with very promising performance, other new gate insulator materials, such as ZrO_2 and AlN could be promising alternatives to explore a better gate insulator suitable for III-N MISFETs.

Further study on traps is also required to characterize the dielectric-related traps to resolve the origins of these traps and seek for viable approaches to engineer these traps, as being exercised in the Silicon World. Optical measurements such as optical DTLS may be more suitable to measure the slow traps than the electrical approaches. A DOE is also required to correlate the ALD deposition variables to the characteristics of traps in III-N MISFETs to explore a better ALD deposition processes. Comprehensive study using electrical and optical measurements with engineered ALD deposition conditions should be performed to complete achieve low-defect high-quality MIS structures in III-N field effect transistors.

REFERENCES

[1] Y. Zhang, "Development of III-Nitride Bipolar Devices: Avalanche Photodiodes, Laser Diodes, and Double-Heterojunction Bipolar Transistors," *Ph.D. dissertation, School Elect. Eng., Georgia Institute of Technology, Atlanta, GA,* 2011.

[2] H. Amano, N. Sawaki, I. Akasaki and Y. Toyoda, "Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer," *Appl. Phys. Lett.,* vol. 48, p. 353, 1986.

[3] B.-T. Liou, S.-H. Yen and Y.-K. Kuo, "Vegard's law deviation in band gaps and bowing parameters of the wurtzite III-nitride ternary alloys," *Proc. SPIE - Int. Soc. Opt. Eng.,* vol. 5628, pp. 296-305, 2005.

[4] V. Kumar, A. Kuliev, T. Tanaka, Y. Otoki and I. Adesida, "High transconductance enhancement-mode AlGaN/GaN HEMTs on SiC substrate," *Electron. Lett.,* vol. 39, pp. 1758-60, Nov. 2003.

[5] W. Lanford, T. Tanaka, Y. Otoki and I. Adesida, "Recessed-gate enhancement-mode GaN HEMT with high threshold voltage," *Electron. Lett.,* Vols. 41, no.7, pp. 449-50, Mar. 2005.

[6] S. Maroldt, C. Haupt, W. Pletschen, S. Mu¨ller, R. Quay, O. Ambacher, C. Schippel and F. Schwierz, "Gate-Recessed AlGaN/GaN Based Enhancement-Mode High Electron Mobility Transistors for High Frequency Operation," *Jpn. J. Appl. Phys.,* Vols. 48, no. 4,, p. 04C083, Apr. 2009.

[7] W. Lim, J.-H. Jeong, H.-B. Lee, J.-H. Lee, S.-B. Hur, J.-K. Ryu, K.-S. Kim, T.-H. Kim, S. Y. Song, W.-G. Hur, S. T. Kim and S. J. Pearton, "Normally-off operation of recessed-gate AlGaN/GaN HFETs for high power applications," *Electrochem. Solid-State Lett.,* vol. 14, no. 5 pp. H205-H207, 2011.

[8] Z. Mouffak, A. Bensaoula and L. Trombetta, "The effects of nitrogen plasma on reactive-ion etching induced damage in GaN," *J. Appl. Phys,* Vols. 95, no. 2, p. 727, Jan 2004..

[9] M. Kato, K. Mikamo, M. Ichimura, M. Kanechika, O. Ishiguro and T. Kachi, "Characterization of plasma etching damage on p-type GaN using Schottky diodes," *J. Appl. Phys.,* vol. 103, p. 093701, 2008.

[10] M. Tajima, J. Kotani and T. Hashizume, "Effects of Surface Oxidation of AlGaN on DC Characteristics of AlGaN/GaN High-Electron-Mobility Transistors," *Jpn. J. Appl. Phys.,* vol. 48, p. 020203, 2009.

[11] S. T. Bradley, S. H. Goss, L. J. Brillson, J. Hwang and W. J. Schaff, "Deep level defects and doping in high Al mole fraction AlGaN," *J. Vac. Sci. Technol. B,* vol. 21, p. 2558, 2003.

[12] B. Yang and P. Fay, "Etch rate and surface morphology control in photoelectrochemical etching of GaN," *J. Vac. Sci. Technol. B,* Vols. 22, no. 4, pp. 1750-1754, Jul. 2004.

[13] C. Youtsey, T. Romano and a. I. Adesida, "Gallium nitride whiskers formed by selective photoenhanced wet etching of dislocations," *Appl. Phys. Lett.,* Vols. 73, no. 6, pp. 797-9, Aug. 1998.

[14] J. A. Bardwell, J. B. Webb, H. Tang, J. Fraser and S. Moisa, "Ultraviolet photoenhanced wet etching of GaN in K2S2O8 solution," *J. Appl. Phys.,* Vols. 89, no. 7, pp. 4142-9, Apr. 2001.

[15] K. Nomoto, T. Tajima, T. Mishima, M. Satoh and T. Nakamura, "Remarkable Reduction of On-Resistance by Ion Implantation in GaN/AlGaN/GaN HEMTs With Low Gate Leakage Current," *IEEE Electron Dev. Lett.,* Vols. 28, no. 11, p. 939, Nov. 2007.

[16] K. P. Lee, A. P. Zhang, G. Dang, F. Ren, J. Han, S. N. G. Chu, W. S. Hobson, J. Lopata, C. R. Abernathy, S. J. Rearson and J. W. Lee, "Self-aligned process for emitter- and base-regrowth GaN HBTs and BJTs," *Solid-State Electron.,* Vols. 45, no. 2, pp. 243-247, 2001.

[17] T. Makimoto, K. Kumakura and N. Kobayashi, "Extrinsic base regrowth of p-InGaN for Npn-type GaN/InGaN heterojunction bipolar transistors," *Jpn. J. Appl. Phys.,* Vols. 43, no. 4B, pp. 1922-1924, Apr. 2004.

[18] T. Huang, X. Zhu and K. M. Lau, "Enhancement-Mode AlN/GaN MOSHFETs on Si Substrate With Regrown Source/Drain by MOCVD," *IEEE Electron Dev. Lett.,* Vols. 33, no. 8, p. 1123, Aug. 2012.

[19] J. Guo, G. Li, F. Faria, Y. Cao, R. Wang, J. Verma, X. Gao, S. Guo, E. Beam, A. Ketterson, M. Schuette, P. Saunier, M. Wistey and D. Jena, "MBE-Regrown Ohmics in InAlN HEMTs With a Regrowth Interface Resistance of 0.05 $\Omega \cdot$ mm," *IEEE Electron Dev. Lett.,* Vols. 33, no. 4, p. 525, Apr. 2012.

[20] Z. Fan, S. N. Mohammad, W. Kim, O. Aktas, A. E. Botchkarev and H. Morkoc, "Very low resistance multilayer Ohmic contact to n-GaN," *Appl. Phys. Lett.,* vol. 68, p. 1672, 1996.

[21] A. Motayed, R. Bathe, M. C. Wood, O. S. Diouf, R. D. Vispute and S. N. Mohammad, "Electrical, thermal, and microstructural characteristics of Ti/Al/Ti/Au multilayer ohmic contacts to n-type GaN," *J. Appl. Phys.,* vol. 93, p. 1087, 2003.

[22] H. K. Cho, T. Hossain, J. W. Bae and I. Adesida, "Characterization of Pd/Ni/Au ohmic contacts on p-GaN," *Solid-State Electron.,* vol. 49, pp. 774-778, 2005.

[23] J. K. Kim, J.-L. Lee, J. W. Lee, H. E. Shin, Y. J. Park and T. Kim, "Low resistance Pd/Au ohmic contacts to p-type GaN using surface treatment," *Appl. Phys. Lett.,* vol. 73, p. 20, Nov. 1998.

[24] A. D. Koehler, N. Nepal, T. J. Anderson, M. J. Tadjer, K. D. Hobart, C. R. E. Jr. and F. J. Kub, "Atomic Layer Epitaxy AlN for Enhanced AlGaN/GaN HEMT Passivation," *Electron Dev. Lett.,* Vols. 34, no. 9, p. 1115, Sep. 2013.

[25] N. Ramanan, B. Lee, C. Kirkpatrick, R. Suri and V. Misra, "Properties of atomic layer deposited dielectrics for AlGaN/GaN device passivation," *Semicond. Sci. Technol.,* Vols. 28, no. 7, p. 074004, 2013.

[26] F. Medjdoub, M. V. Hove, K. Cheng, D. Marcon, M. Leys and S. Decoutere, "Novel E-mode GaN-on-Si MOSHEMT using a selective thermal oxidation," *IEEE Electron Device Lett.,* Vols. 31, no. 9, pp. 948-950, Sep. 2010.

[27] N. Harada, Y. Hori, N. Azumaishi, K. Ohi and T. Hashizume, "Formation of recessed-oxide gate for normally-off AlGaN/GaN high electron mobility transistors

using selective electrochemical oxidation," *Appl. Phys. Exp.,* Vols. 4, no. 2, pp. 021002-1, Feb. 2011.

[28] E. A. Alam, I. Corte´s, M.-P. Besland, A. Goullet, L. Lajaunie, P. Regreny, Y. Cordier, J. Brault, A. Cazarre, K. Isoird, G. Sarrabayrouse and F. Morancho, "Effect of surface preparation and interfacial layer on the quality of SiO2/GaN interfaces," *J. Appl. Phy.*, vol. 109, p. 084511, 2011.

[29] T. Marron, S. Takashima, Z. Li and T. P. Chow, "Impact of annealing on ALD Al2O3 gate dielectric for GaN MOS devices," *Phys. Status Solidi. C,* Vols. 9, no. 3-4, pp. 907-910, 2012.

[30] C. Mizue, Y. Hori, M. Miczek and T. Hashizume, "Capacitance–Voltage Characteristics of Al2O3 /AlGaN/GaN Structures and State Density Distribution at Al2O3/AlGaN Interface," *Jpn. J. Appl. Phys.*, vol. 50, p. 021001, 2011.

[31] W. Snodgrass, W. Hafez, N. Harff and M. Feng, "Pseudomorphic InP/InGaAs Heterojunction Bipolar Transistors (PHBTs) Experimentally Demonstrating fT = 765 GHz at 25°C Increasing to fT = 845 GHz at -55°C," in *Tech. Dig. Int. Electron Device Meeting*, San Francisco, CA, 2006.

[32] M. Urteaga, R. Pierson, P. Rowell, V. Jain, E. Lobisser and M. Rodwe, "130nm InP DG-HBTs with fT > 0.52 THz and fmax > 1.1 THz," in *69th Annual Device Research Conference (DRC)*, Santa Barbara, CA, USA, 2011.

[33] L. McCarthy, P. Kozodoy, M. Rodwell, S. Denbaars and U. K. Mishra, "A first look at AlGaN/GaN HBTs," *Compd. Semicond.,* Vols. 4, no.8, pp. 16-18, 1998.

[34] J. Han, A. Baca, R. Shul, C. Willison, L. Zhang, F. Ren, A. Zhang, G. Dang, S. Donovan, X. Cao, H. Cho, K. Jung, C. Abernathy, S. J. Pearton and R. G. Wilson, "Growth and fabrication of GaN/AlGaN heterojunction bipolar transistor," *Appl. Phys. Lett.*, Vols. 74, no. 18, pp. 2702-2704, 1999.

[35] J. J. Huang, M. Hattendorf, M. Feng, D. Lambert, B. Shelton, M. Wong, U. Chowdhury, T. Zhu, H. Kwon and R. D. Dupuis, "Graded-emitter AlGaN/GaN heterojunction bipolar transistors," *IEEE Electron. Lett.,* Vols. 36, no. 14, pp. 1239-1240, 2000.

[36] X. Cao, G. Dang, A. Zhang, F. Ren, J. M. V. Hove, J. J. Klaassen, C. J. Polley, A. M. Wowchak, P. P. Chow, D. J. King, C. R. Abernathy and S. J. Pearton, "High current, common-base GaN/AlGaN heterojunction bipolar transistors," *Electrochem. Solid-State Lett.,* Vols. 3, no. 3, pp. 144-146, 2000.

[37] H. G. Xing and U. K. Mishra, "Temperature dependent I-V characteristics of AlGaN/GaN HBTs and GaN BJTs," *Int. J. High Speed Electron. Syst.,* Vols. 14, no. 3, pp. 819-824, Sep. 2004.

[38] D. Keogh, P. Asbeck, T. Chung, J. Limb, D. Yoo, J.-H. Ryou, W. Lee, S. C. Shen and R. D. Dupuis, "High current gain InGaN/GaN HBTs with 300C operating temperature," *Electron. Lett.*, vol. 42, p. 661, 2006.

[39] A. Nishikawa, K. Kumakura and T. Makimoto, "Temperature dependence of current-voltage characteristics of npn-type GaN/InGaN double heterojunction bipolar transistors," *Appl. Phys. Lett.*, vol. 91, p. 133514, 2007.

[40] L. McCarthy, I. Smorchkova, P. Fini, M. Rodwell, J. Speck, S. DenBaars and U. K.

Mishra, "Small signal RF performance of AIGaN/GaN heterojunction bipolar transistors," *Electron. Lett.*, vol. 38, p. 144, Jan. 2002.

[41] K. Kumakura, T. Makimoto and N. Kobayashi, "Low-resistance nonalloyed ohmic contact to p-type GaN using strained InGaN contact layer," *Appl. Phys. Lett.*, vol. 79, no. 16, pp. 2588-2590, Oct. 2001.

[42] T. Makimoto, K. Kumakura and N. Kobayashi, "High current gains obtained by InGaN/GaN double heterojunction bipolar transistors with p-InGaN base," *Appl. Phys. Lett.*, vol. 79, no. 3, pp. 380-381, 2001.

[43] K. Kumakura, T. Makimoto and N. Kobayashi, "Mg-acceptor activation mechanism and transport characteristics in p-type InGaN grown by metalorganic vapor phase epitaxy," *J. Appl. Phys.*, vol. 93, no. 6, p. 3370, 2003.

[44] D. J. Kim, D. Y. Ryu, N. A. Bojarczuk, J. Karasinski, S. Guha, S. H. Lee and J. H. Lee, "Thermal activation energies of Mg in GaN:Mg measured by the Hall effect and admittance spectroscopy," *J. Appl. Phys.*, vol. 88, no. 5, p. 2564, Sep. 2000.

[45] H. Jiang and J. Lin, "AlGaN and InAlGaN alloys-epitaxial growth, optical and electrical properties and applications," *Opto-electronics review*, vol. 10, no. 4, pp. 271-286, 2002.

[46] K. Kumakura and T. Makimoto, "High performance pnp AlGaN/GaN heterojunction bipolar transistors on GaN substrates," *Appl. Phys. Lett.*, vol. 92, no. 15, pp. 153509-1, Apr. 2008.

[47] L. S. McCarthy, P. Kozodoy, M. J. W. Rodwell, S. P. DenBaars and U. K. Mishra, "AlGaN/GaN heterojunction bipolar transistor," *IEEE Electron Device Lett.*, vol. 20, no. 6, pp. 277-279, 1999.

[48] M. Feng and J. Laskar, "On the speed and noise performance of direct ion implanted GaAs MESFET's," *IEEE Trans. Electron Dev., vol. 40, no. 1, pp. 9-17, 1993.*, Vols. 40, no. 1, pp. 9-17, Jan. 1993.

[49] J. Zolper, A. Baca, M. Sherwin and R. Shul, "High performance GaAs JFET with shallow implanted Cd-gate," *Electron. Lett., vol. 31, no. 11, pp. 923-4, May 1995*, vol. 31. no. 11, pp. 923-4, May 1995.

[50] D.-H. Kim, B. Brar and J. A. d. Alamo, "fT = 688 GHz and fmax = 800 GHz in Lg = 40 nm In0.7Ga0.3As MHEMTs with gm_max > 2.7 mS/μm," in *Tech. Dig Int. Electron. Dev. Meeting*, Washington, D.C., USA, 2011.

[51] S. Razavi, S. Zahiri and S. Hosseini, "A novel 4H–SiC MESFET with recessed gate and channel," *Superlattices Microstruct.*, vol. 60, pp. 516-23, Aug. 2013.

[52] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, p. 3222, Mar. 1999.

[53] J. Kolnik, I. H. Oiuzman, K. E. Brennana, R. Wang, P. P. Ruden and Y. Wang, "Electronic transport studies of bulk zincblende and wurtzite phases of GaN based on an ensemble Monte Carlo calculation including a full zone band structure," *J. Appl. Phys.*, Vols. 78, no. 2, p. 15, Jul. 1995.

[54] J. W. Chung, W. E. Hoke, E. M. Chumbes and T. Palacios, "AlGaN/GaN HEMT With 300-GHz fmax," *IEEE Electron Dev. Lett.,* Vols. 31, no. 3, p. 195, Mar. 2010.

[55] S. Bouzid-Driad, H. Maher, N. Defrance, V. Hoel, J.-C. D. Jaeger, M. Renvoise and P. Frijlink, "AlGaN/GaN HEMTs on Silicon Substrate With 206-GHz fmax," *IEEE Electron Dev. Lett., vol. 34, no. 1, Jan. 2013.,* Vols. 34, no. 1, p. 36, Jan. 2013.

[56] K. Shinohara, D. Regan, A. Corrion, D. Brown, S. Burnham, P. Willadsen, I. Alvarado-Rodriguez, M. Cunningham, C. Butler, A. Schmitz, S. Kim, B. Holden, D. Chang, V. Lee, A. Ohoka, P. Asbeck and M. Micovic, "Deeply-scaled self-aligned-gate GaN DH-HEMTs with ultrahigh cutoff frequency," in *Tech. Dig. Int. Electron Device Meeting*, Washington, DC, USA, 2011.

[57] T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. P. DenBaars, J. S. Speck and U. K. Mishra, "High-power AlGaN/GaN HEMTs for Ka-band applications," *IEEE Electron Device Lett.,* Vols. 26, no. 11, pp. 781-783, Nov. 2005.

[58] M. Micovic, A. Kurdoghlian, P. Hashimoto, M. Hu, M. Antcliffe, P. J. Willadsen, W. S. Wong, R. Bowen, I. Milosavljevic, A. Schmitz, M. Wetzel and D. H. Chow, "GaN HFET for W-band power applications," in *Tech. Dig. Int. Electron Device Meeting*, San Francisco, CA, USA, 2006.

[59] A. Maekawa, T. Yamamoto, E. Mitani and S. Sano, "A 500W Push-Pull AlGaN/GaN HEMT amplifier for L-Band High Power Application," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.,*, 2006.

[60] S. Rajan, A. Chini, M. H. Wong, J. S. Speck and U. K. Mishra, "N-polar GaN/AlGaN/GaN high electron mobility transistors," *J. Appl. Phys.,* vol. 102, p. 044501, 2007.

[61] S. Dasgupta, Nidhi, D. F. Brown, F. Wu, S. Keller, J. S. Speck and U. K. Mishra, "Ultralow nonalloyed Ohmic contact resistance to self-aligned N-polar GaN high electron mobility transistors by In(Ga)N regrowth," *Appl. Phys. Lett.,* vol. 96, p. 143504, 2010.

[62] F. Medjdoub, M. Zegaoui, D. Ducatteau, N. Rolland and P. Rolland, "First AIN/GaN HEMTs power measurement at 18 GHz on Silicon substrate," in *2011 69th Annual Device Research Conference (DRC),* Santa Barbara, CA, USA, 2011.

[63] R. Wang, G. Li, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena and H. Xing, "210-GHz InAlN/GaN HEMTs with Dielectric-Free Passivation," *IEEE Electron Dev. Lett., vol. 32, no. 7, July 2011,* Vols. 32, no. 7, pp. 892 - 894, Jul. 2011.

[64] H. Sun, A. R. Alt, H. Benedickter, C. R. Bolognesi, E. Feltin, J.-F. Carlin, M. Gonschorek and N. Grandjean, "Ultrahigh-Speed AlInN/GaN High Electron Mobility Transistors Grown on (111) High-Resistivity Silicon with fT =143GHz," *Appl. Phys. Exp.,* vol. 3, p. 094101, 2010.

[65] K. Shinohara, A. Corrion, D. Regan, I. Milosavljevic, D. Brown, S. Burnham, P. J. Willadsen, C. Butler, A. Schmitz, D. Wheeler, A. Fung and M. Micovic, "220 GHz fT and 400 GHz fMAX in 40-nm GaN DH-HEMTs with re-grown ohmic," in *in Tech. Dig. Int. Electron Dev. Meeting ,* San Francisco, CA, USA, 2010.

[66] H. Yu, L. McCarthy, S. Rajan, S. Keller, S. Denbaars, J. Speck and U. Mishra, "Ion Implanted AlGaN–GaN HEMTs With Nonalloyed Ohmic Contacts," *IEEE Electron Dev. Lett.,* vol. 26, no. 5, pp. 283-285, May 2005.

[67] S. Yoshida, J. Li, T. Wada and H. Takehara, "High-Power AlGaN/GaN HFET with a Lower On-state Resistance and a Higher Switching Time for an Inverter Circuit," in *Proc. IEEE 2003 Int. Symp. Power Semicond. Dev. ICs (ISPSD)*, Cambridge, UK, 2003.

[68] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito and K. Tsuda, "ON-Resistance Modulation of High Voltage GaN HEMT on Sapphire Substrate Under High Applied Voltage," *IEEE Electron Dev. Lett.,* Vols. 28, no. 8, p. 676, Aug. 2007.

[69] N. Ikeda, S. Kaya, J. Li, Y. Sato, S. Kato and S. Yoshida, "High power AlGaN/GaN HFET with a high breakdown voltage of over 1.8 kV on 4 inch Si substrates and the suppression of current collapse," in *Proc. 20th Int. Symp. Power Semicond. Dev. IC's*, Oralando, FL, USA, May 2008.

[70] C. Zhou, W. Chen, E. L. Piner and K. J. Chen, "Self-Protected GaN Power Devices with Reverse Drain Blocking and Forward Current Limiting Capabilities," in *Proc. 22nd Int. Symp. Power Semicond. Dev. & ICs*, Hiroshima, Japan, 2010.

[71] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka and D. Ueda, "Gate Injection Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation," *IEEE Trans. Electron Dev.,* Vols. 54, no. 12, p. 3393, 2007.

[72] O. Hilt, F. Brunner, E. Cho, A. Knauer, E. Bahat-Treidel and J. Würfl, "Normally-off High-Voltage p-GaN Gate GaN HFET with Carbon-Doped Buffer," in *Proc. 23rd Int. Symp. Power Semicond. Devices & IC's*, San Diego, CA, USA, May 2011.

[73] L. Yuan, H. Chen, Q. Zhou, C. Zhou and K. J. Chen, "A Novel Normally-off GaN Power Tunnel Junction FET," in *Proc. 23rd Int. Symp. Power Semicond. Dev. & IC's*, San Diego, CA, USA, May 2011.

[74] D. S. Lee, B. Lu, M. Azize, X. Gao, S. Guo, D. Kopp, P. Fay and T. Palacios, "Impact of GaN Channel Scaling in InAlN/GaN HEMTs," in *Tech. Dig. Int. Electron Device Meeting* , Washington, DC, USA, 2011.

[75] H. Kambayashi, Y. Satoh, S. Ootomo, T. Kokawa, T. Nomura, S. Kato and T.-S. P. Chow, "Over 100 A operation normally-off AlGaN/GaN hybrid MOS-HFET on Si substrate with high-breakdown voltage," *Solid-State Electronics*, vol. 54, pp. 660-664, 2010.

[76] J.-P. Ao, K. Nakatani, K. Ohmuro, M. Sugimoto, C.-Y. Hu, Y. Sogawa and Y. Ohno, "GaN Metal–Oxide–Semiconductor Field-Effect Transistor with Tetraethylorthosilicate SiO2 Gate Insulator on AlGaN/GaN Heterostructure," *Jpn. J. Appl. Phys.*, vol. 49, p. 04DF09, 2010.

[77] T. Oka and T. Nozawa, "AlGaN/GaN Recessed MIS-Gate HFET With High-Threshold-Voltage Normally-Off Operation for Power Electronics Applications," *IEEE Electron Dev. Lett.,* Vols. 29, no. 7, pp. 668-670, Jul. 2008.

[78] Y. Z. Yue, Y. Hao, J. Zhang, J. Ni, W. Mao, Q. Feng and L. Liu, "AlGaN/GaN MOS-HEMT With HfO2 Dielectric and Al2O3 Interfacial Passivation Layer

Grown by Atomic Layer Deposition," *IEEE Electron Dev. Lett, vol. 29, no. 8, Aug. 2008,* Vols. 29, no. 8, p. 838, Aug. 2008.

[79] S. Abermann, G. Pozzovivo, J. Kuzmik, G. Strasser, D. Pogany, J.-F. Carlin, N. Grandjean and E. Bertagnolli, "MOCVD of HfO2 and ZrO2 high-k gate dielectrics for InAlN/AlN/GaN MOS-HEMTs," *Semicond. Sci. Technol.,* vol. 22, pp. 1272-1275, 2007.

[80] B. Luo, J. W. Johnson, J. Kim, R. M. Mehandru, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abernathy, S. J. Pearton, A. G. Baca, R. D. Briggs, R. J. Shul, C. Monier and J. Han, "Influence of MgO and Sc2O3 passivation on AlGaN/GaN high-electron-mobility transistors," *Appl. Phy. Lett.,* Vols. 80, no. 9, p. 4, Mar. 2002.

[81] T.-Y. Wu, S.-K. Lin, P.-W. Sze, J.-J. Huang, W.-C. Chien, C.-C. Hu, M.-J. Tsai and Y.-H. Wang, "AlGaN/GaN MOSHEMTs With Liquid-Phase-Deposited TiO2 as Gate Dielectric," *IEEE Trans. Electron Dev., vol. 56, no. 12, Dec. 2009,* Vols. 56, no. 12, p. 2911, Dec. 2009.

[82] Y.-L. Chiou, C.-S. Lee and C.-T. Lee, "AlGaN/GaN metal-oxide-semiconductor high-electron mobility transistors with ZnO gate layer and (NH4)2Sx surface treatment," *Appl. Phys. Lett.,* vol. 97, p. 032107, 2010.

[83] M. Kanamura, T. Ohki, T. T. Kikkawa, K. Imanishi, T. Imada and N. Hara, "High Current Operation of Enhancement-Mode GaN MIS-HEMTs with Triple Cap Structure Using Atomic Layer Deposited Al2O3 Gate Insulator," in *Dig. 67th Dev. Res. Conf. (DRC)* , 2009 .

[84] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder and J. C. M. Hwang, "GaN metal-oxide-semiconductor high-electron-mobility-transistor with atomic layer deposited Al2O3 as gate dielectric," *Appl. Phy. Lett.,* vol. 86, p. 063501, 2005.

[85] H. Zhou, G. I. Ng, Z. H. Liu and S. Arulkumaran, "Improved Device Performance by Post-Oxide Annealing in Atomic-Layer-Deposited Al2O3/AlGaN/GaN Metal–Insulator–Semiconductor High Electron Mobility Transistor on Si," *Appl. Phys. Exp.,* vol. 4, p. 104102, 2011.

[86] A. P. Zhang, L. B. Rowland, E. B. Kaminsky, V. Tilak, J. C. Grande, J. Teetsov, A. Vertiatchikh and L. F. Eastman, "Correlation of device performance and defects in AlGaN/GaN high-electron mobility transistors," *J. Electron. Mater.,* vol. 32, p. 388, May 2003.

[87] Z.-Q. Fang, D. C. Look, D. H. Kim and I. Adesida, "Traps in AlGaN GaN SiC heterostructures studied by deep level transient spectroscopy," *Appl. Phys. Lett.,* vol. 87, p. 182115, 2005.

[88] A. M. Armstrong, A. A. Allerman, A. G. Baca and C. A. Sanchez, "Sensitivity of on-resistance and threshold voltage to buffer-related deep level defects in AlGaN/GaN high electron mobility transistors," *Semicond. Sci. Technol.,* vol. 28, p. 074020, 2013.

[89] D. Bisi, M. Meneghini, C. d. Santi, A. Chini, M. Dammann, P. Brückner, M. Mikulla, G. Meneghesso and E. Zanoni, "Deep-Level Characterization in GaN HEMTs-Part I: Advantages and Limitations of Drain Current Transient Measurements," *IEEE Trans. Electron Dev., vol. 60, no. 10, Oct. 2013,* vol. 60, no.

10, pp. 3166 - 3175, Oct. 2013.

[90] J. Joh and J. A. d. Alamo, "A Current-Transient Methodology for Trap Analysis for GaN High Electron Mobility Transistors," *IEEE Trans. Electron Dev., vol. 58, no. 1, Jan 2011,* vol. 58, no. 1, pp. 132-140, Jan. 2011.

[91] A. Fontserè, A. Pérez-Tomás, P. Godignon, J. Millán, H. D. Vleeschouwer, J. M. Parsey and P. Moens, "Wafer scale and reliability investigation of thin HfO2 AlGaN/GaN MIS-HEMTs," *Microelectron. Reliab.,* vol. 52, p. 2220, 2012.

[92] W. Choi, H. Ryu, N. Jeon, M. Lee, H.-Y. Cha and K.-S. Seo, "Improvement of Vth Instability in Normally-Off GaN MIS-HEMTs Employing PEALD-SiNx as an Interfacial Layer," *IEEE Electron Dev. Lett.,* vol. 35, no. 1, pp. 30-32, Jan. 2014.

[93] W. Liu, Foundamentals of III-V Devices - HBTs, MESFETS and HFETs/HEMTs, John Wiley & Sons, Inc, 1999.

[94] W. Liu and J. J. S. Harris, "Diode Ideality Factor for Surface Recombination Current in AlGaAs/GaAs Heterojunction Bipolar Transistors," *IEEE Trans. Electron Dev.,* vol. 39, no. 12, pp. 2726-2732, Dec. 1992.

[95] S.-C. Shen, R. D. Dupuis, Z. Lochner, Y.-C. Lee, T.-T. Kao, Y. Zhang, H.-J. Kim and J.-H. Ryou, "Working toward high-power GaN/InGaN heterojunction bipolar transistors," *Semicond. Sci. Technol.,* vol. 28, p. 074025, 2013.

[96] G. Gonzalez, Microwave Transistor Amplifiers: Analysis and Design, Prentice Hall, 1996.

[97] S. J. Mason, "Power gain in feedback amplifier," *Trans. IRE Professional Group on Circuit Theory,* Vols. CT-1, no. 2, pp. 20-25, June 1954.

[98] M. Vaidyanathan and D. L. Pulfrey, "Extrapolated fmax of Heterojunction Bipolar Transistors," *IEEE TRans. Electron Dev.,* vol. 46, no. 2, p. 301, Feb. 1999.

[99] K. Kurishima, "An Analytic Expression of fmax for HBTs," *IEEE Trans. Electron Dev.,* vol. 43, no. 12, p. 2074, Dec. 1996.

[100] Z. Lochner, H. Kim, S. Choi, Y.-C. Lee, Y. Zhang, S.-C. Shen, J.-H. Ryou and R. D. Dupuis, "Growth and characterization of NpN heterojunction bipolar transistors with In0.03Ga0.97N and In0.05Ga0.95N bases," *J. Crystal Growth,* vol. 315, pp. 278-282, 2011.

[101] Y. Zhang, J.-H. Ryou, R. D. Dupuis and S.-C. Shen, "A surface treatment technique for III-V device fabrication," in *Dig. 2008 Int. Conf. Compound Semicond. Manuf. Technol.*, Chicago, IL,, 2008.

[102] S. A. Smith, C. A. Wolden, M. D. Bremser, A. D. Hanser, R. F. Davis and W. V. Lampert, "High rate and selective etching of GaN, AlGaN, and AlN using an inductively coupled plasma," *Appl. Phys. Lett.,* vol. 71, no. 25, p. 3631, 1997.

[103] D. Kent, K. Lee, A. Zhang, B. Luo, M. Overberg, C. Abernathy, F. Ren, K. Mackenzie, S. Pearton and Y. Nakagawa, "Effect of N2 plasma treatments on dry etch damage in n- and p-type GaN," *Solid-State Electron,* vol. 45, p. 457, 2001.

[104] J.-O. Song, J. S. Kwak, Y. Park and T.-Y. Seong, "Ohmic and degradation mechanisms of Ag contacts on p-type GaN," *Appl. Phys. Lett.,* vol. 86, p. 062104, 2005.

[105] Z. Lochner, H.-J. Kim, S. Choi, Y.-C. Lee, Y. Zhang, J.-H. Ryou, S.-C. Shen and

R. Dupuis, "Growth and characterization of npn heterojunction bipolar transistors with InxGa1-xN bases," in *15th Int. Conf. Metal Organic Vapor Phase Epitaxy*, Lake Tahoe, NV, May 2010.

[106] Y.-C. Lee, Y. Zhang, H.-J. Kim, S. Choi, Z. Lochner, R. D. Dupuis, J.-H. Ryou and S.-C. Shen, "High-current-gain direct-growth GaN/InGaN double heterojunction bipolar transistors," *IEEE Trans. Electron Dev.*, vol. 57, no. 11, pp. 2964-2969, Nov. 2010.

[107] T. Henderson, V. Ley, T. Kim, T. Moise and D. Hill, "Hydrogen-related burn-in in GaAs/AlGaAs HBTs and implications for reliability," in *Tech. Dig. IEEE Int. Electron Dev. Meeting (IEDM)*, New York, USA, 1996.

[108] M. Borgarino, R. Plana, S. Delage, H. Blanck, F. Fantini and J. Graffeuil, "Early variations of the base current in In/C-doped GaInP-GaAs HBTs," in *IEEE 36th Annu. Int. Reliab. Phys. Symp.*, Reno, NV, USA, 1998.

[109] N. Bovolon, R. Schultheis, J. E. Muller and P. Zwicknagl, "Analysis of the short-term DC-current gain variation during high current density-low temperature stress of AlGaAs/GaAs heterojunction bipolar transistors," *IEEE Trans. Electron Dev.*, vol. 47, no. 2, pp. 274-281, Feb. 2000.

[110] S. Nakamura, N. Iwasa, M. Senoh and T. Mukai, "Hole compensation mechanism of P-type GaN films," *Jpn. J. Appl. Phys.*, vol. 31, no. 5, pp. 1258-1266, May 1992.

[111] S. J. Pearton, C. R. Abernathy, C. B. Vartuli, J. W. Lee, J. D. MacKenzie, R. G. Wilson, R. J. Shul, F. Ren and J. M. Zavada, "Unintentional hydrogenation of GaN and related alloys during processing," *J. Vac. Sci. Technol. A*, vol. 14, p. 8310835, May 1996.

[112] S. M. Sze, Physics of Semiconductor devices, 2nd ed., Wiley, 1981.

[113] Z. Lochner, H.-J. Kim, Y.-C. Lee, Y. Zhang, S. Choi, S.-C. Shen, P. D. Yoder, J.-H. Ryou and R. D. Dupuis, "Npn-GaN/InGaN/GaN heterohunction bipolar transistor on free-standing GaN substrate," *Appl. Phys. Lett.*, vol. 99, p. 193501, 2011.

[114] Y.-C. Lee, Y. Zhang, Z. Lochner, H.-J. Kim, J. H. Ryou, R. D. Dupuis and S.-C. Shen, "Ultra-high-power characteristics of GaN/InGaN HBTs," in *2011 9th Int. Conf. Nitride Semicond.*, Glasgow, UK, 2011.

[115] J. Yuan, J. D. Cressler, R. Krithivasan, T. Thrivikraman, M. H. Khater, D. C. Ahlgren, A. J. Joseph and J.-S. Rieh, "On the performance limits of cryogenically operated SiGe HBTs and its relation to scaling for terahertz speeds," *IEEE Trans. Electron Dev.*, vol. 56, no. 5, p. 1007, 2009.

[116] F. H.-F. Chau, B. J.-F. Lin, Y. Chen, M. Kretschmar, C.-P. Lee, N.-L. L. Wang, X. Sun, W. Ma, S. Xu and P. Hu, "Reliability study of InGaP/GaAs HBT for 28V operation," in *Tech. Dig. IEEE Compd. Semicond. Integr. Circuit Symp.*, San Antonio,TX, USA, 2006.

[117] Y. Zeng, O. Ostinelli, R. Lövblom, A. R. Alt, H. Benedickter and C. R. Bolognesi, "400-GHz InP/GaAsSb DG-HBTs with low-noise microwave performance," *IEEE Electron Dev. Lett.*, vol. 31, no. 10, pp. 1122-1124, Oct. 2010.

[118] K. Kumakura and T. Makimoto, *Jpn. J. Appl. Phys.*, vol. 46, no. 4B, p. 2338–2340,

2007.

[119] S.-C. Shen, Y.-C. Lee, H.-J. Kim, Y. Zhang, S. Choi, R. D. Dupuis and J.-H. Ryou, "Surface leakage in GaN/InGaN double heterojunction bipolar transistors," *IEEE Electron Dev. Lett.*, vol. 30, no. 11, pp. 1119-1121, Nov. 2009.

[120] J. Penn and C. Moore, "GaAs MMlC Probe Measurements and Calibration Techniques," in *39th ARFTG Conf. Dig.*, Albuquerque, NM, USA, June 1992.

[121] S.-C. Shen, R. D. Dupuis, Y.-C. Lee, H.-J. Kim, Y. Zhang, Z. Lochner, P. D. Yoder and J.-H. Ryou, "GaN/InGaN Heterojunction Bipolar Transistors with fT > 5 GHz," *IEEE Electron Dev. Lett.*, vol. 32, no. 8, pp. 1065-1067, Aug. 2011.

[122] M. Feng, S.-C. Shen, D. Caruth and J.-J. Huang, "Device technologies for RF front-end circuits in next-generation wireless communications," *Proc. IEEE*, vol. 92, pp. 354-75, 2004.

[123] Y.-C. Lee, H. J. Kim, Y. Zhang, S. Choi, R. D. Dupuis, J. H. Ryou and S. C. Shen, "High-performance GaN/InGaN heterojunction bipolar transistors using a direct-growth approach," *phys. stat. sol. (c)*, vol. 7, pp. 1970-1973, 2010.

[124] R. D. Dupuis, S.-C. Shen, Z. M. Lochner, H.-J. Kim, Y.-C. Lee, Y. Zhang, C.-Y. Wang and J.-H. Ryou, "III-Nitride Heterojunction Field-Effect Transistors and Heterojunction Bipolar Transistors for Next-Generation Power Electronics," *ECS Trans.*, vol. 41, no. 8, pp. 73-85, 2011.

[125] Z. Lochner, H.-J. Kim, S. Choi, Y.-C. Lee, Y. Zhang, S.-C. Shen, J.-H. Ryou and R. D. Dupuis, "Growth and characterization of NpN heterojunction bipolar transistors with In0.03Ga0.97N and In0.05Ga0.95N bases," *J. Crystal Growth*, vol. 315, no. 1, pp. 278-282, 2011.

[126] Y. Zhang, Y.-C. Lee, Z. Lochner, H. Kim, S. Choi, J.-H. Ryou, R. D. Dupuis and S.-C. Shen, "High-Performance GaN/InGaN double heterojunction bipolar transistors on with power density > 240 kW/cm2," *Physica Status Solidi (c)*, vol. 8, no. 7-8, pp. 2451-2453, 2011.

[127] Y.-C. Lee, Y. Zhang, Z. M. Lochner, H.-J. Kim, J.-H. Ryou, R. D. Dupuis and S.-C. Shen, "GaN/InGaN heterojunction bipolar transistors with ultra-high d.c. power density (>3MW/cm2)," *Phys. Status Solidi A*, vol. 209, no. 3, pp. 497-500, 2012.

[128] R. Dupuis, H. J. Kim, Y.-C. Lee, Z. Lochner, M.-H. Ji, T.-T. Kao, J.-H. Ryou, T. Detchphrom and S.-C. Shen, "III-N High-Power Bipolar Transistors," *ECS Trans.*, vol. 58, no. 4, pp. 261-267, 2013.

[129] Y.-C. Lee, S.-C. Shen, H.-J. Kim, Y. Zhang, S. Choi, J.-H. Ryou and R. D. Dupuis, "High performance GaN/InGaN heterojunction bipolar transistors using a direct-growth approach," in *The 8th International Conference on Nitride Semiconductors (ICNS-8)*, Jeju, Korea, 2009.

[130] Y.-C. Lee, H.-J. Kim, Y. Zhang, S. Choi, R. D. Dupuis, J.-H. Ryou and S.-C. Shen, "A Study on the Base Recombination Current in Direct-Growth npn GaN/InGaN DHBTs," in *Digest of the 2010 CSMANTECH Conference*, Portland, OR, USA, 2010.

[131] Y. Zhang, Y.-C. Lee, Z. Lochner, H. Kim, S. Choi, J.-H. Ryou, R. D. Dupuis and S.-C. Shen, "GaN/InGaN double heterojunction bipolar transistors on sapphire

substrates with current gain > 100, JC > 7.2 kA/cm2, and power density > 240 kW/cm2," in *International Workshop on Nitride Semiconductors 2010 (IWN-2010)*, Tampa, Florida, USA, 2010.

[132] Y. Zhang, Y.-C. Lee, Z. Lochner, H. J. Kim, J.-H. Ryou, R. D. Dupuis and S.-C. Shen, "GaN/InGaN Heterojunction Bipolar Transistors with Collector Current Density > 20 kA/cm2," in *Digest of the 2011 CSMANTECH Conference*, Palm Springs, CA, USA, 2011.

[133] Y.-C. Lee, Y. Zhang, Z. Lochner, H.-J. Kim, J. H. Ryou, R. D. Dupuis and S.-C. Shen, "Ultra-high-power characteristics of GaN/InGaN HBTs," in *the 9th International Conference on Nitride Semiconductors (ICNS-9)*, Glasgow, UK, 2011.

[134] Z. Z. Lochner, H.-J. Kim, Y. Zhang, Y.-C. Lee, S. Choi, S.-C. Shen, P. D. Yoder, J.-H. Ryou and R. D. Dupuis, "Epitaxial and characterization of npn-GaN/InGaN/GaN heterojunction bipolar transistors on foreign and native substrates," in *ACCGE-18/OMVPE-15*, Monterey, CA, USA, 2011.

[135] Y.-C. Lee, T.-T. Kao, J. Kim, M.-H. Ji, T. Detchprohm, R. D. Dupuis and S.-C. Shen, "Device Degradation Mechanisms in npn GaN/InGaN Heterojunction Bipolar Transistors," in *2014 GOMACTech conference*, Charleston, SC, USA, 2014.

[136] Y.-C. Lee, T.-T. Kao, J. Kim, M.-H. Ji, T. Detchphrom, R. D. Dupuis and S.-C. Shen, "Npn GaN/InGaN Heterojunction Bipolar Transistors Using a Palladium-Based Contact," in *Digest of the 2014 CSMANTECH conference*, Denver, CO, USA, 2014.

[137] J. Pusl, J. Brown, J. Shealy, M. Hu, A. E. Schmitz, D. P. Docter, M. Case, M. Thompson and L. Nguyen, "High-efficiency GaAs-based pHEMT power amplifier technology for 1-18 GHz," in *Proc. MTT Symp.*, San Francisco, CA, USA, Jun. 1996.

[138] G. Meneghesso, A. Mion, A. Neviani, M. Matloubian, J. Brown, M. Hafizi, T. Liu, C. Canali, M. Pavesi, M. Manfredi and E. Zanoni, "Effects of channel quantization and temperature on off-state and on-state breakdown in composite channel and conventional InP-based HEMTs," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 1996.

[139] F. Bernardini and V. Fiorentini, "Spontaneous Polarization and Piezoelectric Constants of III-V Nitrides," *Phys. Rev. B*, vol. 56, no. 16, pp. R10024-R10027, 1997.

[140] F. Bernardini, V. Fiorentini and D. Vanderbilt, "Accurate Calculation of Polarization-Related Quantities in Semiconductors," *Phys. Rev. B*, vol. 63, no. 19, p. 193201, 2001.

[141] F. Bernardini and V. Fiorentini, "Spontaneous polarization and piezoelectric constants of III-V nitrides," *Phys. Rev. B*, vol. 56, no. 16, p. R10024, 1997.

[142] A. E. Romanov, T. J. Baker, S. Nakamura, J. S. Speck and E. U. Group, "Strain-induced polarization in wurtzite III-nitride semipolar layers," *J. Appl. Phys.*, vol. 100, p. 023522, 2006.

[143] H. Morkoç, Handbook of Nitride Semiconductors and Devices, Volume 1,

Materials Properties, Physics and Growth, Wiley, 2008.

[144] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, A. J. Sierakowski, W. J. Schaff, L. F. Eastman, R. Dimitrov, A. Mitchell and M. Stutzmann, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *J. Appl. Phys.,* vol. 87, p. 334, 2000.

[145] J. H. Edgar, Properties of Group III Nitrides, London: INSPEC, 1994.

[146] C. Wood and D. Jena, Polarization Effects in Semiconductors : From Ab Initio Theory to Device Applications, Boston, MA: Springer, 2008.

[147] K. Tsubouchi, K. Sugai and N. Miskoshiba, "Zero temperature coefficient surface-acoustic-wave devices using epitaxial AlN film," in *1982*, San Diego, CA, USA, Proc. IEEE Ultrason. Symp..

[148] A. F. Wright, "Elastic properties of zinc-blende and wurtzite AlN, GaN, and InN," *J. Appl. Phys.,* vol. 82, p. 2833, 19978.

[149] C. Deger, E. Born, H. Angerer, O. Ambacher, M. Stutzmann, J. Hornsteiner, E. Riha and G. Fischerauer, "Sound velocity of AlxGa1-xN thin films obtained by surface acoustic-wave measurements," *Appl. Phys. Lett.,* vol. 72, p. 2400, 1998.

[150] L.-Y. Su, F. Lee and J. J. Huang, "Enhancement-mode Gan-based high-electron mobility transistors on the Si substrate with a P-Type GaN cap layer," *IEEE Trans. Electron. Dev.,* vol. 61, no. 2, pp. 460-465, Feb. 2014.

[151] L. Shen, T. Palacios, C. Poblenz, A. Corrion, A. Chakraborty, N. Fichtenbaum, S. Keller, S. P. Denbaars, J. S. Speck and U. K. Mishra, "Unpassivated High Power Deeply Recessed GaN HEMTs With Fluorine-Plasma Surface Treatment," *IEEE Electron Dev. Lett.,* vol. 27, no. 4, pp. 214-216, Apr. 2006.

[152] M. J. Wang, L. Yuan, K. J. Chen, F. J. Xu and B. Shen, "Diffusion mechanism and the thermal stability of fluorine ions in GaN after ion implantation," *J. Appl. Phys.,* vol. 105, p. 083519, 2009.

[153] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda and I. Omura, "Recessed-Gate Structure Approach Toward Normally Off High-Voltage AlGaN/GaN HEMT for Power Electronics Applications," *IEEE Trans. Electron Dev.,* vol. 53, no. 2, p. 356, Feb. 2006.

[154] M. J. Uren, K. J. Nash, R. S. Balmer, T. Martin, E. Morvan, N. Caillas, S. L. Delage, D. Ducatteau, B. Grimbert and J. C. D. Jaeger, "Punch-Through in Short-Channel AlGaN/GaN HFETs," *IEEE Trans Electron Dev.,* vol. 53, no. 2, p. 395, Feb. 2006.

[155] G. Xie, E. Xu, J. Lee, N. Hashemi, W. T. Ng, B. Zhang and F. Y. Fu, "Breakdown Voltage Enhancement for Power AlGaN/GaN HEMTs with Air-bridge Field Plate," in *2012 24th Int. Symp. Power Semicond. Dev. IC's (ISPSD 2012)*, Bruges, Belgium, 2012.

[156] Y. Ando, K. Ishikura, K. Yamanoguchi, K. Asano and H. Takahashi, "Theoretical and Experimental Study of Inverse Piezoelectric Effect in AlGaN/GaN Field-Plated Heterostructure Field-Effect Transistors," *IEEE Trans. Electron Dev.,* vol. 59, no. 12, p. 3350, Dec. 2012.

[157] S. Choi, H. J. Kim, Z. Lochner, J. Kim, R. D. Dupuis, A. M. Fischer, R. Juday, Y. Huang, T. Li, J. Y. Huang, F. A. Ponce and J.-H. Ryou, "Origins of unintentional incorporation of gallium in AlInN layersduring epitaxial growth, part I: Growth of AlInN on AlN and effectsof prior coating," *J. Crystal Growth,* vol. 388, pp. 137-142, 2014.

[158] J. Kim, Z. Lochner, M.-H. Ji, S. Choi, H. J. Kim, J. S. Kim, R. D. Dupuis, A. M. Fischer, R. Juday, Y. Huang, T. Li, J. Y. Huang, F. A. Ponce and J.-H. Ryou, "Origins of unintentional incorporation of gallium in InAlN layers during epitaxial growth, part II: Effects of underlying layers and growth chamber conditions," *J. Crystal Growth,* vol. 388, pp. 143-149, 2014.

[159] M. Gonschorek, J.-F. Carlin, E. Feltin, M. A. Py and N. Grandjean, "High electron mobility lattice matched AlInN/ GaN field-effect transistor heterostructures," *Appl. Phys. Lett.,* vol. 89, p. 062106, 2006.

[160] Y.-C. Lee, C.-Y. Wang, T.-T. Kao and S.-C. Shen, "Threshold Voltage Control of Recessed-Gate III-N HFETs Using an Electrode-less Wet Etching Technique," in *Proc. Int. Conf. Compd. Semicond. Manuf. Technol.* , Boston, MA, USA, 2012.

[161] S. Ootomo, T. Hashizume and H. Hasegawa, "Surface passivation of AlGaN/GaN heterostructures using an ultrathin Al2O3 layer," *Phys. Status Solidi A,* vol. 188, no. 1, pp. 371-374, Nov. 2001.

[162] R. Carli and C. Bianchi, "XPS analysis of gallium oxides," *Appl. Surf. Sci.,* vol. 74, no. 1, pp. 99-102, Jan. 1994.

[163] N. Ikeda, J. Li and S. Yoshida, "Normally-off operation power AlGaN/GaN HFET," in *2004 Int. Symp. Power Semicond. Dev. ICs,* , Kitakyushu, Japan, 2004.

[164] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka and D. Ueda, "Normally-off AlGaN/GaN Transistor with RonA = 2.6mΩcm2 and BVds = 640V Using Conductivity Modulation," in *Tech. Dig. Int. Electron Device Meeting*, San Francisco, CA, USA, 2006.

[165] W. Chen, K.-Y. Wong and K. J. Chen, "Single-chip boost converter using monolithically integrated AlGaN/GaN lateral field-effect rectifier and normally off HEMT," *IEEE Electron Dev. Lett.,* vol. 30, no. 5, p. 430, May 2009.

[166] T. Imada, M. Kanamura and T. Kikkawa, "Enhancement-Mode GaN MIS-HEMTs for Power Supplies," in *2010 Int. Power Electron. Conf.*, Singapore, 2010.

[167] H. Kambayashi, Y. Satoh, Y. Niiyama, T. Kokawa, M. Iwami, T. Nomura and S. Kato, "Enhancement-mode GaN Hybrid MOS-HFETs on Si substrates with Over 70 A operation," in *Proc. 2009 Int. Symp. Power Semicond. Dev. ICs*, Barcelona, Spain, 2009.

[168] H. Kambayashi, Y. Satoh, T. Kokawa, N. Ikeda, T. Nomura and S. Kato, "High field-effect mobility normally-off AlGaN/GaN hybrid MOS-HFET on Si substrate by selective area growth technique," *Solid-State Electron.,* vol. 56, p. 163, 2011.

[169] A. L. Corrion, M. Chen, R. Chu, S. D. Burnham, S. Khalil, D. Zehnder, B. Hughes and K. Boutros, "Normally-off Gate-Recessed AIGaN/GaN-on-Si Hybrid MOS-HFET with Al2O3 Gate Dielectric," in *2011 69th IEEE Dev. Res. Conf.*, Santa Barbara, CA, USA, 2011.

[170] R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes and K. Boutros, "Normally Off GaN-on-Si Field-Effect Transistors With Low Dynamic ON-Resistance," *IEEE Electron Dev. Lett.*, vol. 32, no. 5, pp. 632-634, May 2011.

[171] N. Ikeda, R. Tamura, T. Kokawa, H. Kambayashi, Y. Sato, T. Nomura and S. Kato, "Over 1.7 kV normally-off GaN hybrid MOS-HFETs with a lower on-resistance on a Si substrate," in *Proc. 23rd Int. Symp. Power Semicond. Dev. ICs*, Osaka, Japan, 2011.

[172] O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel and J. Würfl, "Normally-off AlGaN/GaN HFET with p-type GaN Gate and AlGaN Buffer," in *Proc. 22nd Int. Symp. Power Semicond. Dev. ICs*, Hiroshima, Japan, 2010.

[173] Y. Ohmaki, M. Tanimoto, S. Akamatsu and T. Mukai, "Enhancement-mode AlGaN/AlN/GaN high electron mobility transistor with low on-state resistance and high breakdown voltage," *J. Appl. Phys.*, vol. 45, p. L1168, 2006.

[174] F. Medjdoub, J. Derluyn, K. Cheng, M. Leys, S. Degroote, D. Marcon, D. Visalli, M. V. Hove, M. Germain and G. Borghs, "Low On-Resistance High-Breakdown Normally Off AlN/GaN/AlGaN DHFET on Si Substrate," *IEEE Electron Dev. Lett.*, vol. 31, no. 2, pp. 111-113, Feb. 2010.

[175] R. Dimitrov, V. Tilak, W. Yeo, B. Green, H. Kim, J. Smart, E. Chumbes, J. R. Shealy, W. Schaff, L. F. Eastman, C. Miskys, O. Ambacher and M. Stutzmann, "Influence of oxygen and methane plasma on the electrical properties of undoped AlGaN/GaN heterostructures for high power transistors," *Solid-State Electron.*, vol. 44, p. 1361, 2000.

[176] C.-Y. Hu and T. Hashizume, "Reliability Improvement Achieved by N2O Radical Treatment for AIGaN/GaN Heterojunction Field-Effect Transistors," in *Proc. 70th IEEE Dev. Res. Conf.*, University Park, TX, USA, 2012.

[177] S. Huang, Q. Jiang, S. Yang, C. Zhou and K. J. Chen, "Effective Passivation of AlGaN/GaN HEMTs by ALD-Grown AlN Thin Film," *IEEE Electron Dev. Lett.*, vol. 33, no. 4, p. 516, Apr. 2012.

[178] H. Sun, A. R. Alt, H. Benedickter, E. Feltin, J.-F. Carlin, N. R. G. M. Gonschorek and C. R. Bolognesi, "205-GHz (Al,In)N/GaN HEMTs," *IEEE Electron Dev. Lett.*, vol. 31, no. 9, p. 957, Sep. 2010.

[179] D. S. Lee, O. Laboutin, Y. Cao, W. Johnson, E. Beam, A. Ketterson, M. Schuette, P. Saunier, D. Kopp, P. Fay and T. Palacios, "317 GHz InAlGaN/GaN HEMTs with extremely low on-resistance," *Phys. Status Solidi C*, vol. 10, no. 5, pp. 827-830, 2013.

[180] R. Wang, G. Li, G. Karbasian, J. Guo, F. Faria, Z. Hu, Y. Yue, J. Verma, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena and H. Xing, "InGaN Channel High-Electron-Mobility Transistors with InAlGaN Barrier and fT=fmax of 260/220 GHz," *Appl. Phys. Exp.*, vol. 6, pp. 016503-1, 2013.

[181] K. Shinohara, D. Regan, I. Milosavljevic, A. L. Corrion, D. F. Brown, P. J. Willadsen, C. Butler, A. Schmitz, S. Kim, V. Lee, A. Ohoka, P. M. Asbeck and M. Micovic, "Electron Velocity Enhancement in Laterally Scaled GaN DH-HEMTs With fT of 260 GHz," *IEEE Electron Dev. Lett.*, vol. 32, no. 8, p. 1074, Aug. 2011.

[182] D. S. Lee, J. W. Chung, H. Wang, X. Gao, S. Guo, P. Fay and T. Palacios, "245-

GHz InAlN/GaN HEMTs With Oxygen Plasma Treatment," *IEEE Electron Dev. Lett.*, vol. 32, no. 6, p. 755, June 2011.

[183] Y. Yue, Z. Hu, J. Guo, B. Sensale-Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena and H. Xing, "InAlN/AlN/GaN HEMTs With Regrown Ohmic Contacts and fT of 370 GHz," *IEEE Electron Dev. Lett.*, vol. 33, no. 7, p. 988, Jul. 2012.

[184] D. F. Brown, A. Williams, K. Shinohara, A. Kurdoghlian, I. Milosavljevic, P. Hashimoto, R. Grabar, S. Burnham, C. Butler, P. Willadsen and M. Micovic, "W-Band Power Performance of AlGaN/GaN DHFETs with Regrown n+ GaN Ohmic Contacts by MBE," in *Dig. of 2011 IEEE Int. Electron Dev. Meeting (IEDM)*, Washington, DC, USA, Dec. 2011.

[185] D. Marti, C. R. Bolognesi, Y. Cordier, M. Chmielowska and M. Ramdani, "RF Performance of AlGaN/GaN High-Electron-Mobility Transistors Grown on Silicon (110)," *Appl. Phys. Exp.*, vol. 4, pp. 064105-1, 2011.

[186] M. Higashiwaki, T. Mimura and T. Matsui, "AlN/GaN Insulated-Gate HFETs Using Cat-CVD SiN," *IEEE Electron Dev. Lett.*, vol. 27, no. 9, p. 719, Sep .2006.

[187] R. Wang, G. Li, G. Karbasian, J. Guo, B. Song, Y. Yue, Z. Hu, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena and H. Xing, "Quaternary Barrier InAlGaN HEMTs With fT/fmax of 230/300 GHz," *IEEE Electron Dev. Lett.*, vol. 34, no. 3, p. 378, Mar. 2013.

[188] D. S. Lee, X. Gao, S. Guo and T. Palacios, "InAlN/GaN HEMTs With AlGaN Back Barriers," *IEEE Electron Dev. Lett.*, vol. 32, no. 5, p. 617, May 2011.

[189] S.-C. Shen, Y.-C. Lee, C.-Y. Wang and T.-T. Kao, "Threshold Voltage Control of III-Nitride Field-Effect Transistor Using Electrode-less Photon-Assisted Wet Etching Technique". USA Patent US Provisional 61/552,257 (GTRC ID: 5805), 17 Oct. 2011.

[190] S.-C. Shen, Y.-C. Lee, C.-Y. Wang, T.-T. Kao and F. Hébert, "Low-resistivity Si/Al-based Alloyed Metal Contacts for III-Nitride Semiconductors". USA Patent Georgia Tech Research Corporation (GTRC ID: 5869), 17 Oct. 2011.

[191] S.-C. Shen, Y.-C. Lee, C.-Y. Wang, T.-T. Kao and F. Hébert, "Recessed-Gate III-N Field-Effect Transistor with Etching Stop Layer". USA Patent Georgia Tech Research Corporation (GTRC ID: 5931), 2 Feb. 2012.

[192] Y.-C. Lee, T.-T. Kao, J. J. Merola and S.-C. Shen, "A Remote-Oxygen-Plasma Surface Treatment Technique for III-Nitride Heterojunction Field-Effect Transistors," *IEEE Trans. Electron Dev., vol. 61, no. 2, Feb 2014*, vol. 61, no. 2, pp. 493 - 497, Feb. 2014.

[193] S. Choi, H. J. Kim, Z. Lochner, Y. Zhang, Y.-C. Lee, S.-C. Shen, J.-H. Ryou and R. D. Dupuis, "Threshold voltage control of InAlN/GaN heterostructure field-effect transistors for depletion- and enhancement-mode operation," *Appl. Phys. Lett.*, vol. 96, p. 243506, 2010.

[194] J. Kuzmık, G. Konstantinidis, S. Harasek, Š. Haščık, E. Bertagnolli, A. Georgakilas and D. Pogany, "ZrO2/(Al)GaN metal–oxide–semiconductor structures : characterization and application," *Semicond. Sci. Technol.*, vol. 19, pp. 1364-1368, 2004.

[195] A. Kawano, S. Kishimoto, Y. Ohno, K. Maezawa, T. Mizutani, H. Ueno, T. Ueda and T. Tanaka, "AlGaN/GaN MIS-HEMTs with HfO2 gate insulator," *phys. stat. sol. (c),* vol. 4, no. 7, pp. 2700-2703, 2007.

[196] S. Ozaki, T. Ohki, M. Kanamura, N. Okamoto and T. Kikkaw, "Effect of oxidant source on threshold voltage shift of AlGaN/HaN MIS-HEMTs using ALD-Al2O3 gate insulator films," in *Tech. Dig. 2012 Comp. Semicond. Manufac. Tech.* , Boston, MA, USA, 2012.

[197] H. Zhou, G. I. Ng, Z. H. Liu and S. Arulkumaran, "Improved Device Performance by Post-oxide Annealing in Atomic-layer-deposited AI2O3/AIGaN/GaN Metal-insulator-semiconductor High Electron Mobility Transistor on Si," *Appl. Phys. Exp.* , vol. 4, no. 10, p. 104102, Oct. 2011.

[198] M. Ťapajna and J. Kuzmík, "A comprehensive analytical model for threshold voltage calculation in GaN based metal-oxide-semiconductor high-electron-mobility transistors," *Appl. Phys. Lett.,* vol. 100, p. 113509, 2012.

[199] P. Krispin, "Single-level interface states in semiconductor structures investigated by admittance spectroscopy," *Appl. Phys. Lett.,* vol. 70, no. 11, p. 1432, 1997.

[200] J. F. Chen, N. C. Chen and H. S. Liu, "Characterizations of deep levels in SnTe-doped GaSb by admittance spectroscopy," *Appl. Phys. Lett.,* vol. 69, no. 13, p. 1891, 1996.

[201] E. J. Miller, X. Z. Dang, H. H. Wieder, P. M. Asbeck, E. T. Yu, G. J. Sullivan and J. M. Redwing, "Trap characterization by gate-drain conductance and capacitance dispersion studies of an AlGaNÕGaN heterostructure field-effect transistor," *J. Appl. Phys., vol. 87, no. 11, Jun. 2000,* vol. 87, no. 11, pp. 8070-8073, Jun. 2000.

[202] O. Mitrofanov and M. Manfra, "Mechanisms of gate lag in GaN/AlGaN/GaN high electron mobility transistors," *Superlatt. Microstruc.,* vol. 34, pp. 33-53, 2003.

[203] G. Meneghess, M. Meneghini, D. Bisi, I. Rossetto, A. Cester, U. K. Mishra and E. Zanoni, "Trapping phenomena in AlGaN/GaN HEMTs: a study based on pulsed and transient measurements," *Semicond. Sci. Technol.,* vol. 28, p. 074021, 2013.

[204] D. V. Lang, "Deep-level transient spectroscopy: A new method to characterize traps in semiconductors," *J. Appl. Phys.,* vol. 45, no. 7, p. 3023, 1974.

[205] W. I. Lee, T. C. Huang, J. D. Guo and M. S. Feng, "Effects of column III alkyl sources on deep levels in GaN grown by organometallic vapor phase epitaxy," *Appl. Phys. Lett.,* vol. 67, p. 1721, 1995.

[206] F. D. Auret, S. A. Goodman, F. K. Koschnick, J.-M. Spaeth, B. Beaumont and P. Gibart, "Electrical characterization of two deep electron traps introduced in epitaxially grown n- GaN during He-ion irradiation," *Appl. Phys. Lett.,* vol. 73, p. 3745, 1998.

[207] Z.-Q. Fang, L. Polenta, J. W. Hemsky and D. C. Look, "Deep centers in as-grown and electron-irradiated n-GaN," in *Proc. 2000 Int. Semicond. Insul. Mat. Conf.,* Canberra, ACT, Australia, 2000.

[208] D. K. Johnstone, M. Ahoujja, Y. K. Yeo, R. L. Hengehold and L. Guido, "Deep Centers and Their Capture Barriers in MOCVD-Grown GaN," in *Proc. Mat. Res. Soc. Symp.,* Boston, MA, USA, 2002.

[209] G. A. Umana-Membreno, J. M. Dell, T. P. Hessler, B. D. Nener, G. Parish, L. Faraone and U. K. Mishra, "60 Co gamma-irradiation-induced defects in n-GaN," *Appl. Phys. Lett.*, vol. 80, p. 4354, 2002.

[210] T. Okino, M. Ochiai, Y. Ohno, S. Kishimoto, K. Maezawa and T. Mizutani, "Drain Current DLTS of AlGaN–GaN MIS-HEMTs," *IEEE Electron Dev. Lett., vol. 25, no. 8, Aug. 2004*, vol. 25, no. 8, pp. 523-525, Aug. 2004.

[211] C. B. Soh, S. J. Chua, H. F. Lim, D. Z. Chi, W. Liu and S. Tripathy, "Identification of deep levels in GaN associated with dislocations," *J. Phys., Condens. Matter.*, vol. 16, no. 34, pp. 6305-6315, 2004.

[212] A. R. Arehart, A. Corrion, C. Poblenz, J. S. Speck, U. K. Mishra, S. P. DenBaars and S. A. Ringel, "Comparison of deep level incorporation in ammonia and rf-plasma assisted molecular beam epitaxy n-GaN films," *phys. stat. sol. (c),* vol. 5, no. 6, pp. 1750-1752, 2008.

[213] M. Tapajna, R. J. T. Simms, Y. Pei, U. K. Mishra and M. Kuball, "Integrated Optical and Electrical Analysis: Identifying Location and Properties of Traps in AlGaN/GaN HEMTs During Electrical Stress," *IEEE Electron Dev. Lett., vol. 31, no. 7, July 2010*, vol. 31, no. 7, pp. 662-664, Jul. 2010.

[214] A. R. Arehart, A. Sasikumar, G. D. Via, B. Winningham, B. Poling, E. Heller and S. A. Ringe, "Spatially-discriminating trap characterization methods for HEMTs and their application to RF-stressed AlGaN/GaN HEMTs," in *Tech. Dig. IEEE Int. Electron Dev. Meeting*, San Francisco, CA, USA, 2010.

[215] L. Stuchlikova, J. Šebok, J. Rybár, M. Petrus, M. Nemec, L. Harmatha, J. Benkovská, J. Kovác, J. Škriniarová, T. Lalinský, R. Paskiewicz and M. Tlaczala, "Investigation of Deep Energy Levels in Heterostructures based on GaN by DLTS," in *2010 8th Int.Conf.on Adv. Semicond. Dev. & Microsyst. (ASDAM)*, Smolenice, Slovakia, Oct. 2010.

[216] M. Gassoumi, B. Grimbert, C. Gaquiere and H. Maaref, "Evidence of Surface States for AlGaN/GaN /SiC HEMTs Passivated Si3N4 by CDLTS," *Semiconductors*, vol. 46, no. 3, pp. 382-385, 2012.

[217] D. Jin and J. A. Del Alamo, "Impact of high-power stress on dynamic ON-resistance of high-voltage GaN HEMTs," *Microelectron. Reliab.*, vol. 52, no. 12, pp. 2875-2879, Dec. 2012.

[218] S. Chen, U. Honda, T. Shibata, T. Matsumura, Y. Tokuda, K. Ishikawa, M. Hori, H. Ueda, T. Uesugi and T. Kachi, "As-grown deep-level defects in n-GaN grown by metal–organic chemical vapor deposition on freestanding GaN," *J. Appl. Phys.*, vol. 112, p. 053513, 2012.

[219] M. Caesar, M. Dammann, V. Polyakov, P. Waltereit, W. Bronner, M. Baeumler, R. Quay, M. Mikulla and O. Ambacher, "Generation of traps in AlGaN/GaN HEMTs during RF-and DC-stress test," in *IEEE Int. Reliab. Phys. Symp. Proc.*, Anaheim, CA, United states, 2012.

[220] M. Silvestri, M. J. Uren and M. Kuball, "Iron-induced deep-level acceptor center in GaN/AlGaN high electron mobility transistors: Energy level and cross section," *Appl. Phys. Lett.*, vol. 102, p. 073501, 2013.

[221] A. Sasikumar, A. R. Arehart, S. Martin-Horcajo, M. F. Romero, Y. Pei, D. Brown,

F. Recht, M. A. d. Forte-Poisson, F. Calle, M. J. Tadjer, S. Keller, S. P. DenBaars, U. K. Mishra and S. A. Ringel, "Direct comparison of traps in InAlN/GaN and AlGaN/GaN high electron mobility transistors using constant drain current deep level transient spectroscopy," *Appl. Phys. Lett.*, vol. 103, p. 033509, 2013.

[222] A. Fontserè, A. Pérez-Tomás, P. Godignon, J. Millán, H. D. Vleeschouwer, J. M. Parsey and P. Moens, "Wafer scale and reliability investigation of thin HfO2 AlGaN/GaN MIS-HEMTs," *Microelectron. Reliab.*, vol. 52, p. 2220, 2012.

[223] W. Choi, H. Ryu, N. Jeon, M. Lee, H.-Y. Cha and K.-S. Seo, "Improvement of Vth Instability in Normally-Off GaN MIS-HEMTs Employing PEALD-SiNx as an Interfacial Layer," *IEEE Electron Dev. Lett.*, vol. 35, no. 1, pp. 30-32, Jan. 2014.

[224] J. W. Chung, X. Zhao and T. Palacios, "Estimation of Trap Density in AlGaN / GaN HEMTs from Subthreshold Slope Study," in *Proc. 65th Dev. Res. Conf.*, Notre Dame, IN, USA, 2007.

[225] M. Miczek, C. Mizue, T. Hashizume and B. Adamowicz, "Effects of interface states and temperature on the C - V behavior of metal/insulator/AlGaN/GaN heterostructure capacitors," *J. Appl. Phys.*, vol. 103, p. 104510, 2008.

[226] A. Wakejima, A. F. Wilson, S. Mase, T. Joka and T. Egawa, "Evaluation of Electron Trapping Speed of AlGaN/ GaN HEMT With Real-Time Electroluminescence and Pulsed I–V Measurements," *IEEE Trans. Electron Dev.*, vol. 60, no. 10, p. 3183, Oct. 2013.

[227] M. Marso, M. Wolter, P. Javorka, P. Kordos and H. Luth, "Investigation of buffer traps in an AlGaN/GaN/Si high electron mobility transistor by backgating current deep level transient spectroscopy," *Appl. Phys. Lett.*, vol. 82, no. 4, p. 633, 2003.

[228] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. K. Mishra, C. Canali and E. Zanoni, "Surface-Related Drain Current Dispersion Effects in AlGaN–GaN HEMTs," *IEEE Trans. electron. Dev. vol. 51, no. 10, Oct. 2004*, vol. 51, no. 10, p. 1554, Oct. 2004.

[229] M. Choi, J. L. Lyons, A. Janotti and C. G. V. d. Walle, "Impact of carbon and nitrogen impurities in high-k dielectrics on metal-oxide-semiconductor devices," *Appl. Phy. Lett.*, vol. 102, p. 142902, 2013.

[230] Y.-C. Lee, T.-T. Kao and S.-C. Shen, "A Study on Slow Traps in III-Nitride Normally-Off Recessed-Gate Field-Effect Transistors," *IEEE Trans. Electron Dev.*, p. under review, 2014.

[231] Y.-C. Lee, T.-T. Kao and S.-C. Shen, "study on Al2O3 deposition by atomic layer deposition for III-N meta-insulator-semiconductor field-effect transistors," in *Dig. of the 2013 CSMANTECH Conference*, New Orleans, Louisiana, USA, 2013.

[232] Y.-C. Lee, T.-T. Kao, J. J. Merola, C. Lian, D. Wang, D. Hou and S.-C. Shen, "Carrier Trapping Suppression in AlGaN/GaN Heterostructure Using an Oxygen Plasma Treatment Technique," in *5th International Symposium on Growth of III-Nitrides*, Atlanta, GA, USA, 2014.

[233] Y.-C. Lee, T.-T. Kao, J. J. Merola, C. Lian, D. Wang, D. Hou and S.-C. Shen, "Observation on Slow Carrier Trapping in AlGaN/GaN Schottky Barrier Diodes and MIS Capacitors," in *Dig. of the 2014 CSMANTECH Conference*, Denvor, CO, USA, 2014.

[234] Q. Diduck, H.Nie, B. Alvarez, A. Edwards, D.Bour, O. Aktas and D. Disney, "1000V Vertical JFET Using Bulk GaN," *ECS Trans.*, vol. 58, no. 4, pp. 295-298, 2013.